## Output Voltage Adjustment in DC/DC Converters

When the output voltage $\left(\mathrm{V}_{\mathrm{o}}\right)$ of a DC/DC converter must be adjusted in an application, the manufacturer usually specifies the output adjustable voltage range of the converter, typically $5 \%$ to $10 \%$. The manufacturer provides an adjust terminal to be used by the customer for fine adjustment of $\mathrm{V}_{\mathrm{o}}$. For a better understanding of how it works, an error amplifier and reference voltage is shown in Figure 1.

The error OPAM compares the output voltage $\left(\mathrm{V}_{0}\right)$ to a stable reference voltage and generates an error signal for the pulse width modulator (PWM). The PWM adjusts its duty cycle based on the error signal of the OPAM in order to keep $\mathrm{V}_{\mathrm{o}}$ constant under any line, load, and temperature variation.

It should be understood that a DC/DC converter is a linear system and utilizes negative feedback for control and stability. Also, the output accuracy of the converter depends only on the accuracy of the voltage reference, the open loop gain of the error amplifier, and the accuracy of the close loop component (such as R1, R2, RA, and RX in Figure 1). The opto-coupler and the PWM, together with the error OPAM, contribute to the dynamic or transient response of the converter (see References for more details).

Referring to Figure 1, the output voltage with $\mathrm{V}_{0}$ ADJ terminal open, $\mathrm{V}_{\mathrm{o}}$ is given by:

$$
v_{\mathrm{O}}=\left(\frac{R 1}{R 2}+1\right) \mathrm{v}_{\mathrm{REF}}
$$

Eq. 1

When a lower $V_{0}$ is needed, the external $R X$ resistor is placed between $V_{0} A D J$ and $+V_{0}$. The connection reduces the feedback resistor R1 and the new value of the feedback resistor is:

$$
\mathrm{R}^{\prime}=\mathbf{R 1} 1 /(\mathrm{RA}+\mathrm{RX})
$$

$$
\text { Eq. } 2
$$

When a higher $V_{0}$ is required $R X$ is connected between the $\mathrm{V}_{0}$ ADJ terminal and $-\mathrm{V}_{\mathrm{o}} . \mathrm{R}^{\prime}$ is the parallel combination of R2 and the sum of $R A+R X$ :



FIGURE 1. Typical output control stage of a DC/DC converter

Usually, $R A$ is set for the maximum allowed $V_{0}$ by the factory when $R X=0$.
Therefore: $R 2^{\prime}=\frac{R 2(R A)}{R 2+R A} \Rightarrow V_{O}=\left(\frac{R 1}{R 2^{\prime}}+1\right) V_{\text {REF }}$

$$
V_{o}=\left(\frac{R 1+R 2^{\prime}}{R 2^{\prime}}\right) V_{\text {REF }} \quad \frac{V_{0}}{V_{R E F}}=\frac{R 1+R 2^{\prime}}{R 2^{\prime}} \quad R 2^{\prime}=\frac{R 1}{\frac{V_{0}}{V_{\text {REF }}}-1}
$$

$$
\mathrm{R}^{\prime}=\frac{\mathrm{R} 1\left(\mathrm{~V}_{\mathrm{REF}}\right)}{\mathrm{V}_{\mathrm{O}}-\mathrm{V}_{\mathrm{REF}}}
$$

Eq. 4

Substituting $\frac{R 2(R A)}{R 2+R A}$ for R2' in Eq. 4 and solving for RA, we get:

$$
R A=\frac{R 1(R 2)\left(V_{\text {REF }}\right)}{R 2\left(V_{0}-V_{\text {REF }}\right)-R 1\left(V_{R E F}\right)} \quad \text { Eq. } 5
$$

NOTE: $V_{o}$ in Eq. 5 is not the nominal output of the converter, but the new higher $V_{o}$.

## EXAMPLE

Given R1 $=7.5 \mathrm{k}, \mathrm{R} 2=2.5 \mathrm{k}, \mathrm{V}_{\text {REF }}=2.5 \mathrm{~V}, \mathrm{~V}_{\mathrm{O}}$ Nominal $=10 \mathrm{~V}$ :
For $\mathrm{V}_{\mathrm{O}}=11 \mathrm{~V} \quad$ RA from Eq. $5 \cong 18 \mathrm{k} \Omega$

For lower $\mathrm{V}_{\mathrm{o}}$ :

$$
\mathrm{v}_{\mathrm{o}}^{\prime}=\left(\frac{\mathrm{R} 1^{\prime}}{\mathrm{R} 2}+1\right) \mathrm{v}_{\mathrm{REF}}
$$

Eq. 6

$$
\left(\frac{\mathrm{V}_{0}^{\prime}}{\mathrm{VREF}}-1\right)=\frac{\mathrm{R} 1^{\prime}}{\mathrm{R} 2}
$$

Eq. 7

Let $R A+R X=R T$ and $\left(\frac{V_{0}{ }^{\prime}}{V R E F}-1\right)=K$
Then Eq. 7 becomes R1 ${ }^{\prime}=\mathrm{KR} 2$ and from Eq.2:

$$
R 1^{\prime}=\frac{R 1(R T)}{R 1+R T}
$$

Substituting Eq. 8 into Eq. 7 gives: $\frac{\mathrm{R} 1(\mathrm{RT})}{\mathrm{R} 1+\mathrm{RT}}=\mathrm{KR} 2$

$$
R T=\frac{R 1(R 2)}{\frac{R 1}{K}-R 2} \quad \text { Eq. } 9
$$

Using the same values given for the previous example: For $\mathrm{V}_{\mathrm{O}}=\mathrm{V}_{\mathrm{O}}{ }^{\prime}=9 \mathrm{~V}$, then $\mathrm{RT} \cong 47 \mathrm{k}$.
Given $R A=20 k$, then $R X=27 k$.

From the example above, for a $10 \% \mathrm{~V}_{\mathrm{O}}$ trim up ( 10 V to 11 V ) $R A+R X=18 \mathrm{k}$ and for $10 \% \mathrm{~V}_{0}$ trim down ( 10 V to 9 V ) $R A+R X=47 k$. It is obvious that for a given $R A$, the trim down range of the converter is much higher than that of the trim up. In order not to exceed the manufacturer's recommended trim down range, a series resistor with RA is required and its value can be calculated from Eq. 6 through Eq.9.

By adjusting $\mathrm{V}_{0}$, the bias voltages of V 2 , V 3 increase or decrease. The value of V 2 is calculated to be $\mathrm{V} 2 \geq \mathrm{VD} 1$ in order to turn and keep off Q1 under normal operating conditions. When V2 becomes lower than VD1 through the output voltage adjustment, Q1 is ON continuously and the power dissipated in it is $\mathrm{Pd}_{\mathrm{Q} 1}=(\mathrm{V} 1-\mathrm{VD} 1)$ I1, which can cause failure of Q1. If V2 is trimmed higher than the reverse break-


FIGURE 2. Typical bias circuits in a DC/DC converter

You may be wondering why the $\pm 10 \% \mathrm{~V}_{\mathrm{O}}$ ADJ range cannot be exceeded. The answer is simple: it was designed for $\pm 10 \%$ maximum for the following reason:

The circuit in Figure 2 shows the auxiliary bias supplies used in an isolated DC/DC converter. The internal bias voltage for the input L0, D2, C2 and the output L0, D3, C3 are generated through magnetic coupling of the output inductor L0 in Figure 2. The value of V 2 and V 3 with $\mathrm{V}_{\mathrm{o}}$ ADJ open are given by the following equations:

$$
\begin{aligned}
\mathrm{V} 2= & \frac{\mathrm{N} 2}{\mathrm{~N} 1} \mathrm{~V}_{0} \\
& \text { or } \\
\mathrm{V} 2= & \frac{\mathrm{N} 2}{\mathrm{~N} 1}\left(\frac{\mathrm{R} 1}{\mathrm{R} 2}+1\right) \mathrm{V}_{\mathrm{REF}}
\end{aligned}
$$

and

$$
\mathrm{V} 3=\frac{\mathrm{N} 3}{\mathrm{~N} 1} \mathrm{v}_{\text {。 }}
$$

Eq. 11
$\mathrm{V} 3=\frac{\mathrm{N} 3}{\mathrm{~N} 1}\left(\frac{\mathrm{R} 1}{\mathrm{R} 2}+1\right) \mathrm{V}_{\mathrm{REF}}$
down voltage of the $\mathrm{V}_{\mathrm{BE}}$ junction of Q , which is 3 V to 6 V higher than the base voltage of VD1, Q1 will fail.

The output bias voltage V2, which biases the error amplifier and control circuit, is designed for optimum value for switching the synchronous rectifier transistor Q2, Q3. When $\mathrm{V}_{0}$ is adjusted below the specified value, the output of the error OPAM may saturate, which in turn, affects $\mathrm{V}_{\circ}$ line and load regulation.

A lower V3 can also affect the efficiency of the converter if Q2, Q3 are forced to operate longer in their linear region (Ohmic region). When the output voltage trim exceeds the maximum range, it may destroy the output overvoltage protection zener diode D4 and also lower the efficiency by overdriving the gate to source $\mathrm{C}_{\mathrm{GS}}$ of Q2 and Q3.

When a potentiometer is used for fine adjustment of the output, make sure for the initial turn on that the arm is set to the middle. In high output voltage converters, one must take into consideration the power rating of the selected resistor or potentiometer.

## REFERENCES

Pressman, Abraham I. Switching Power Supply Design. Mcgraw-Hill, Inc. 1991.

