DC/DC Converters in Power Sequencing Systems

System power from multiple supply voltages utilize power up/down sequencing to avoid IC latch up, a potential cause of catastrophic failure of a system. Semiconductor companies offer different ICs to address most power system sequencing needs. When multiple DC/DC converters are used in a system, voltage sequencing can be a complex problem to solve. The system designer has to deal not only with the power up/down sequence of multiple ICs, but must also be familiar with most DC/DC converter power up/down sequences, which can vary from manufacturer to manufacturer and from family to family, as well as, for different input voltage ranges within a family. The follow up design tip may provide some assistance to system engineers.

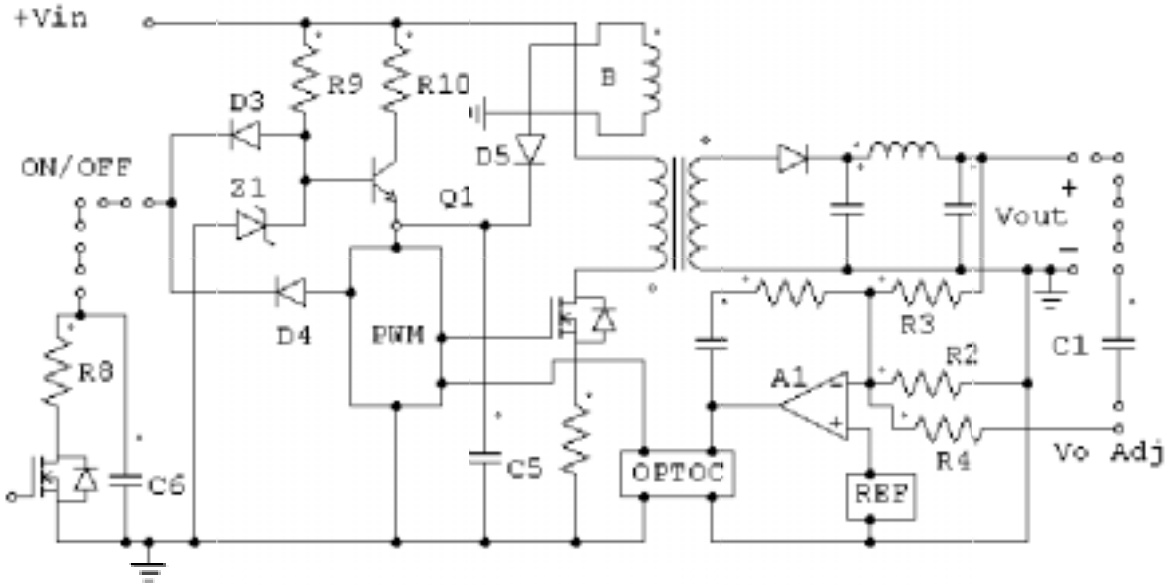

FIGURE 1. Block diagram with positive logic on/off control

$$V_{OUT}\Big|_{t=0} = \left(\frac{R3||R4}{R2}+1\right)VREF$$

$$V_{OUT}\Big|_{t\geq 10} = C1\ R4 = \left(\frac{R3}{R2}+1\right)VREF$$

Figure 1 shows the block diagram of a flyback converter with the bias circuitry for the control IC (PWM) and the feedback loop consistent of the error OPAM A1 and the optocoupler. When Vin is applied while the on/off pin is open, the zener diode Z1, which is biased through R9, holds the base of Q1 at V_z. The emitter voltage of Q1 biases the PWM until the output Vout reaches its steady state and is then forced off by the voltage generated by the boot strap winding B, D5 and C5. Assuming Q1 has a very high current gain ($\beta\rightarrow\infty$), the turn on delay of the converter in Figure 1 is a function of the R10 C5 time constant plus the turn on delay of the PWM. At turn on after the emitter voltage of Q1 exceeds the UVLO threshold of the PWM, the PWM will go through its soft start routine until the output reaches its steady state.

When a longer turn on delay is required to achieve the desired power up sequence, it can be increased with an external capacitor connected between the on/off pin and ground, C6 in Figure 1. See waveforms 2 & 3 in Figure 2. The RC time constant R9 C6 can be tailored with an external component to meet the required sequencing delays of the system. If a longer turn off delay is required, a resistor can be inserted between the drain of Q and the on/off pin of the converter. The R8 C6 time constant will provide the required turn off delay (see waveforms 5 & 6 in Figure 2).

For the converter in Figure 1, the soft start time can be increased by inserting a capacitor between the V_O Adjust pin and $+V_{OUT}$. Inserting C1 in the converter in Figure 1, the output voltage V_{OUT} and turn on delay is given by:

$$V_{OUT}\Big|_{t=0} = [((R3||4)/R2) + 1]V_{REF}$$

After C1 is fully charged:

$$V_{OUT}\Big|_{t\geq 10} = (C1\ R4) = [(R3/R2) + 1)]V_{REF}$$

Most of Beta Dyne's converters are designed using the input biasing and output voltage control base on circuits shown in Figure 1. The flyback converter shown in Figure 1 uses positive logic for the on/off control. In other words, the converter is on if the on/off pin is high or open and off when the on/off pin is low or shorted to the input ground. With few additional components, the converter in Figure 1 becomes the converter shown in Figure 3, which can operate with negative on/off control and its output voltage adjust function is inverted from that in Figure 1.

The turn on/off delays of the converter in Figure 3 can be controlled with a few external components such as D3, D4, R8, R12 and C6, while the soft start function can be increased by connecting C1 between the V_O Adjust pin and output ground. Controlling the turn on/off delays of the power sources in a power sequencing system will provide the most power efficient system because it can eliminate any other control elements in the power path. It will also reduce system compatibility and improve reliability. The component manufacturer most often will provide all the needed information to the system designer, which can speed up the design cycle and eliminate any guessing.

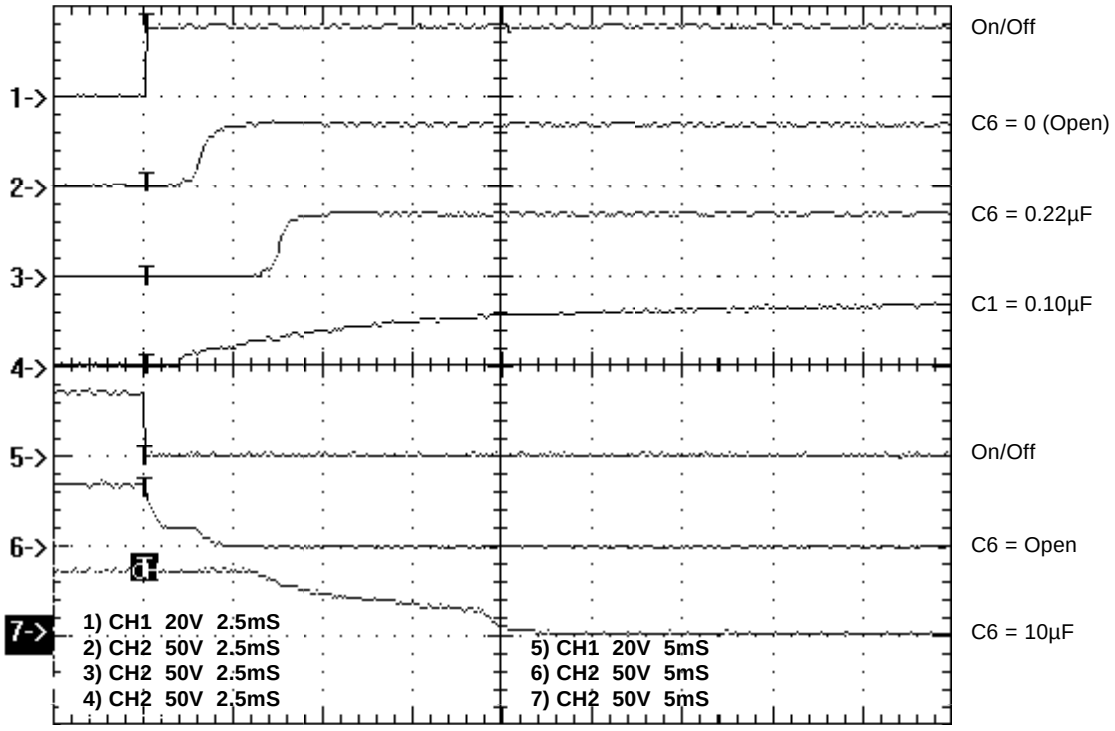

FIGURE 2. Turn on/off delay and soft start waveforms for the DC/DC converter in Figure 1

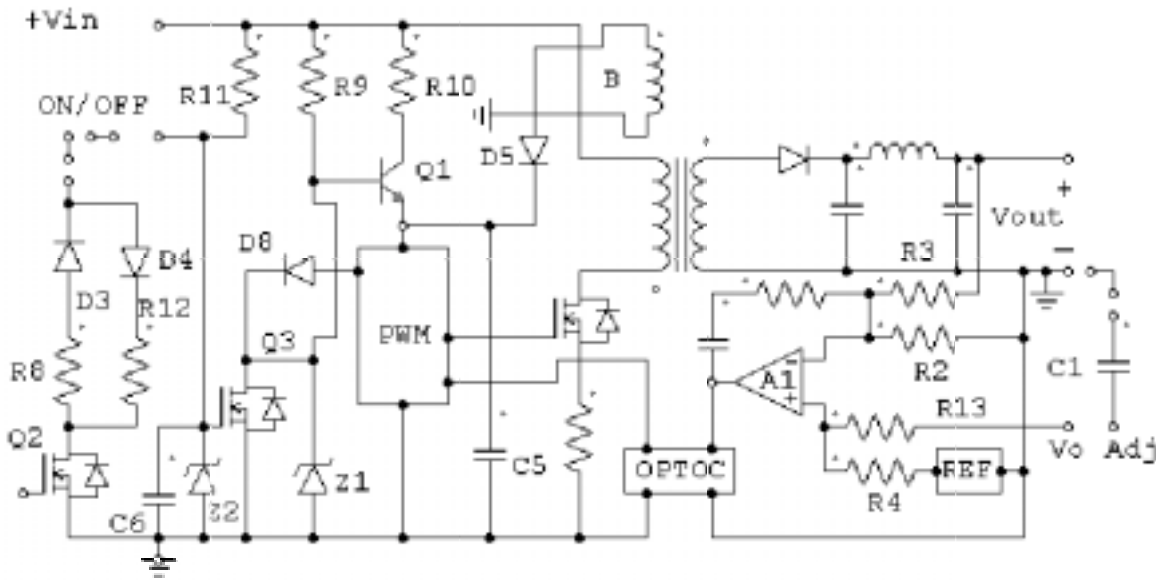

FIGURE 3. Block diagram with negative logic on/off control

$$V_{OUT}\Big|_{t=0} = \left(\frac{R3}{R2}+1\right)\left(\frac{R13}{R13+R4}\right) VREF$$

$$V_{OUT}\Big|_{t\geq 10} = C1(R13+R14) = \left(\frac{R3}{R2}+1\right) VREF$$