DEALING WITH NOISE GENERATED BY A DC/DC CONVERTER

During the conversion process, all DC/DC converters generate unwanted high frequency noise. Over the years designers have used different designs and topologies to minimize and/or eliminate the noise in DC/DC converters. Independent of the design or topology used, cost and performance usually track each other. Cost reduction efforts have influenced the industry up to a point that IC and converter manufacturers design application-specific products to minimize cost. The most commonly used noise reduction component is a low-pass filter at the output and/or input.

Noise in DC/DC converters is known as “conducted noise” or “radiated noise.” Conducted noise is the noise observed on the conductors that connect the converters to the input power source, load or any other control signal. Radiated noise is the same as conducted noise but is radiated to the surrounding space either through the same connecting conductors or from the internal components due to switching voltage/current and magnetic flux, which are present if no electromagnetic shield is used.

For a better understanding of how internal noise is generated, Figure 1 shows a typical forward converter with most of its parasitic element. On the primary side, the parasitic capacitor of the power MOSFET Q1 with LG may cause high frequency ringing on the drain of Q1 while the leakage inductance (L_i) of T1 may generate a high-voltage spike on the drain. A series gate resistance will eliminate the ringing voltage, and a snubber on the drain of Q1 to ground or V_{IN} will reduce the voltage spike due to L_i.

Another way to reduce the L_i spike and some of the effects of the parasitic capacitance in Q1 is to use zero current switching (ZCS), zero voltage switching (ZVS) or both. The parasitics become part of a resonance network; switching of Q1 takes place when the current through it is zero (ZCS) or when the drain voltage is zero (ZVS). ZCS and ZVS also minimize the power dissipation on Q1. One disadvantage of ZCS and ZVS is the switching frequency modulation required by this technique in order to maintain resonance under load and line variations, which also influence the size of the input filter.

By controlling the slew rate of the voltage (dv/dt) and current (di/dt) in the switching element—in this case, Q1, D1 and D2—high frequency noise can be reduced. By reducing the slew rate, the power dissipation in Q1 increases while the maximum switching frequency is reduced and the required size of the magnetic components increases. Linear Technology offers the LT1683 Low-Noise PWM that can be used for push-pull converters. The capacitance C_D-H_S is the capacitance between the drain and the heat sink, which is formed when the transistor is placed very close to an aluminum plate or metal case in order to minimize the thermal resistance from junction to ambient. (The formed capacitor is proportional to the area of its plates and inversely proportional to the distance between them.)

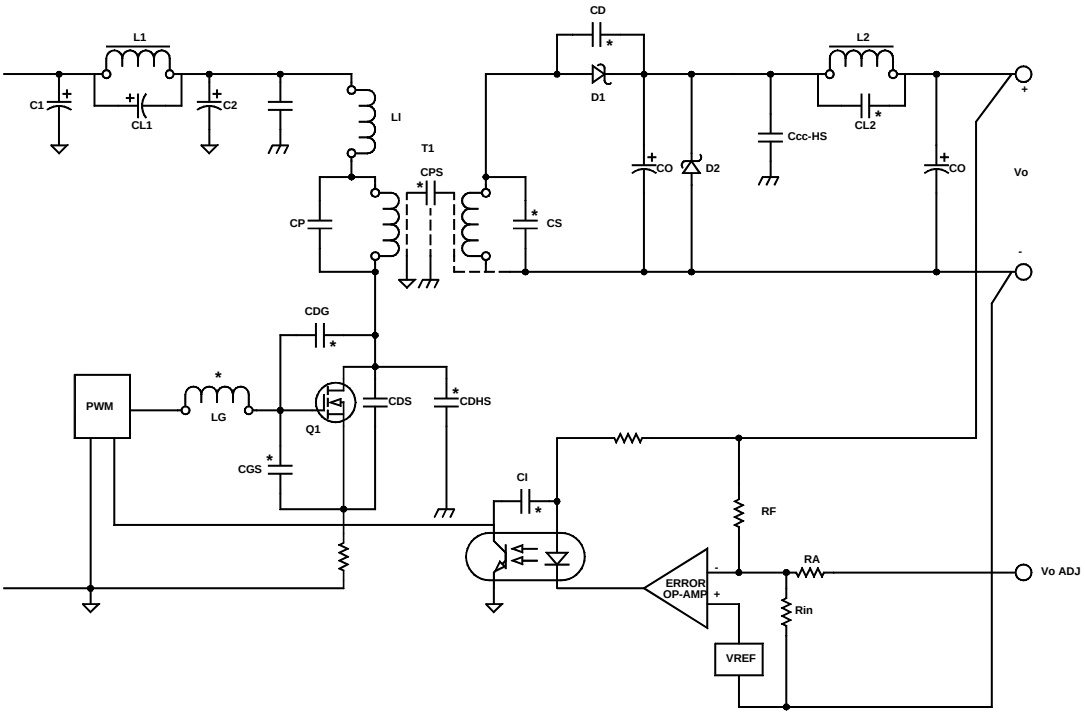

FIGURE 1

The C_D-H_S with $C_{P\text{-}S}$ and C_{CC}-H_S capacitors allow noise to pass between the input and output sections of the converter and may appear at the load; they are also known as input-to-output common-mode noise (CMN).

The interwinding capacitance in the transformer depends on the winding sequence used and the human factor. Different winding sequences will decrease or increase input-to-output capacitance and leakage inductance. For instance, interleaving primary and secondary windings will maximize input-to-output capacitance and will reduce the leakage inductance. In critical applications where $C_{P\text{-}S}$ must be minimized, split bobbins are used to increase the distance between input and output, as well as, to increase input-to-output resistance. For some applications, single open-ended winding shields are used to reduce $C_{P\text{-}S}$ and minimize DC leakage current between input and output (see Reference 3). The reverse recovery time (trr) of output rectifying diodes with the parasitic capacitor generate high frequency oscillations and reduce the converter's efficiency especially in high frequency, high output voltage converters, if trr > 35nS.

The parasitic capacitors of the inductor at the input and output sections of the converter may couple high frequency noise to the power source or the load through CL1 and CL2 respectively. Inductors with multilayer planar windings have relative high parasitic capacitance.

Another technique/design to reduce generated noise is Cuk's converter, whereby integrated magnetics are used to achieve "zero" volts output ripple, input ripple or both (see Reference 1). Assuming a DC/DC converter is a black box that must be inserted in a PCB between the source and the load, and also assuming that the manufacturer specifies all the needed parameters, the system designer can decide if the specified noise of the converter will be acceptable in his/her system. If the specified noise must be reduced at either the input or output of the black box, the following noise reduction circuits may be taken into consideration.

DEALING WITH THE INPUT SIDE

Conducted noise can be reduced using differential and common-mode filters (see Figure 2). Capacitor C1 should be placed as close as possible to the input power pins and its value must be high to eliminate the negative resistance effect on the stability of the converter. A complete analysis of the effects of an input filter in a DC/DC converter can be found in Reference 1; a typical value of C1 is 10µF/A of I_{IN}. As seen in Figure 2, L1 and L2 are in series and the sum of them can be used to calculate the cutoff frequency of the low pass filter formed by L1 + L2 and C1. Capacitors C1, C2 are small ceramic disc capacitors used to bypass the power line noise to chassis ground. Common-mode noise on the power lines is eliminated by the common-mode choke L3, which is typically winded on a toroidal core. The selected core of L3 must not saturate when I_{IN} Max is needed by the converter, which occurs at V_{IN} Min. Magnetics Inc. (www.mag-inc.com) offers downloadable software for common-mode choke designs. Shielded inductors coupled with careful layout will reduce radiated electromagnetic noise. If a multilayer PCB is available, use the inner layers for the power inductor and shield them with ground plain layers.

In Figure 3, a preferred layout is given for both input and output sides of the converter.

NOTE: Common-mode noise in this case is the noise observed between the positive and negative input power conductors, not the "common-mode" noise between input and output sections of the converter.

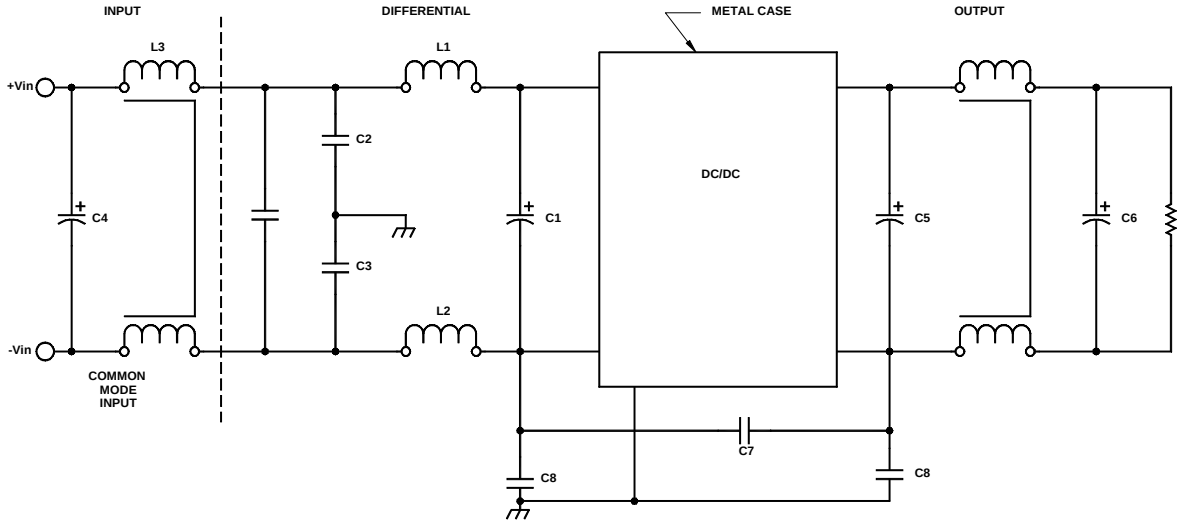

FIGURE 2

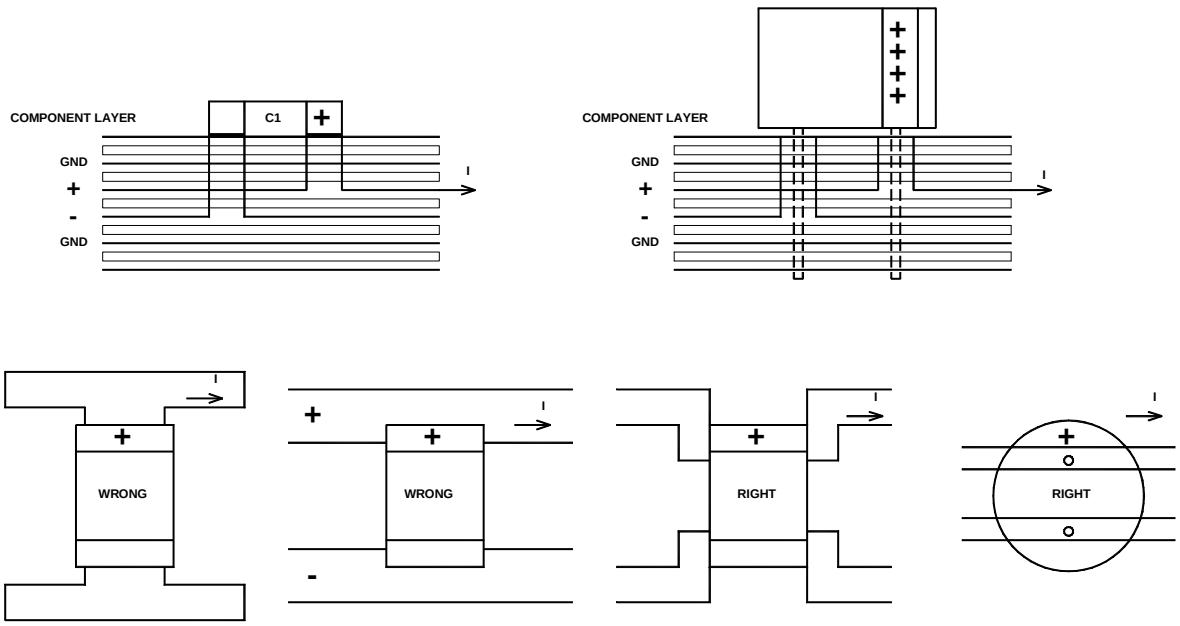

FIGURE 3

NOTE: The current must enter one end of the component and exit at the other. Also when selecting capacitors, check the variation of the capacitance over the operating temperature range.

DEALING WITH OUTPUT NOISE

Referring to Figure 2, a common-mode inductor is used at the output section to reduce output common-mode noise if and when the output ripple is not within acceptable levels and the output current is less than 1A. For higher output currents, the parasitic inductance of the power runs can be used with tantalum capacitors in parallel with 1 to 10µF ceramics to reduce differential and common-mode noise (see Figure 4).

It should also be understood that high inductance values will generate delay and will affect load regulation of the converter. For low output power converters, linear regulators can be used to reduce the output ripple. Low drop out, monolithic linear regulators can also be used. If a monolithic is not available, you can design one of the following regulators or select among Beta Dyne's LN series.

Linear regulators can reduce output ripple by 20 to 40db, but they also reduce the efficiency of the combined power system. To minimize the power dissipated across the pass transistor of the linear regulator, a low drop out regulator must be used. In Figure 5, the output section of a forward converter is followed by a linear regulator. The linear regulator consists of A1, Q2 and a reference voltage VZ.

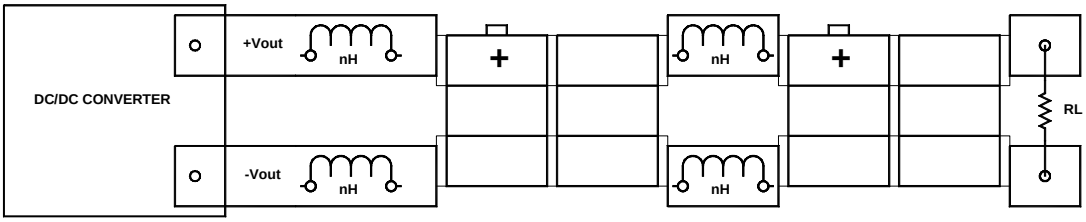

FIGURE 4

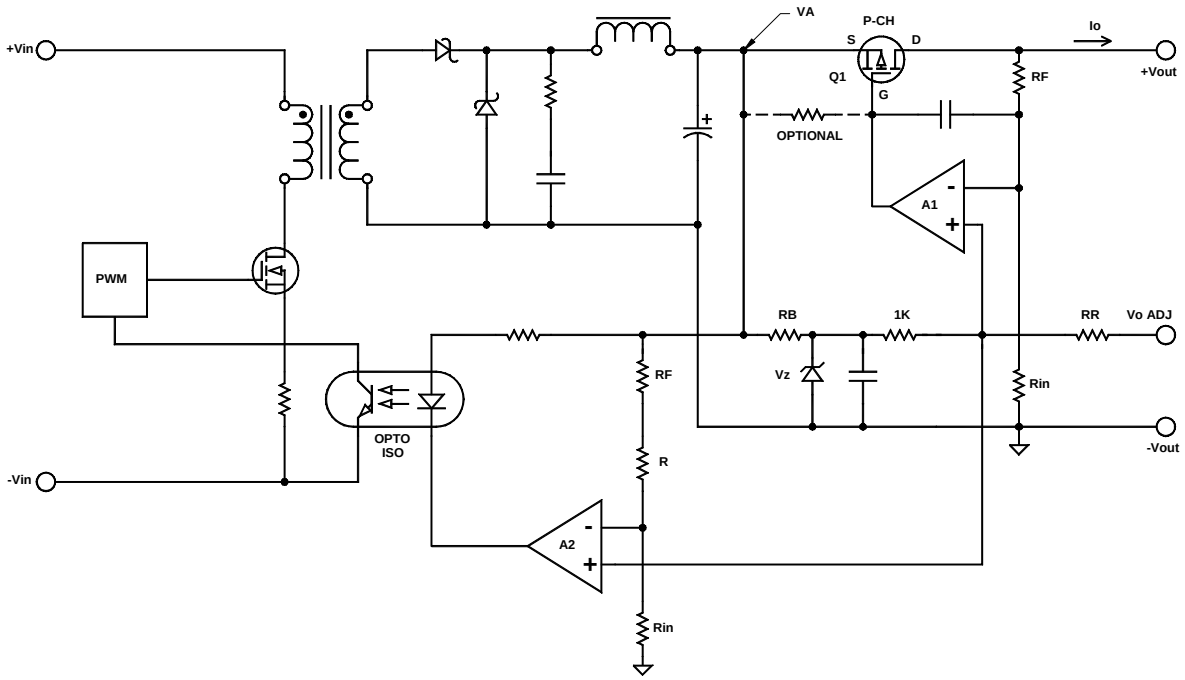

FIGURE 5. Forward DC/DC converter with tracking low drop out linear regulator

Under ideal conditions, the output voltage is given by:

$$V_O = \left(\frac{RF}{R_{IN}} + 1\right)VZ$$

and the output of the forward converter by:

$$VA = \left(\frac{RF+R}{R_1} + 1\right)VZ$$

Solving these two equations for VA-V_O, which is the drop out voltage of the regulator, we get:

$$VA - V_O = \frac{R*VZ}{R_{IN}}$$

$$(VA - V_O)\ \text{minimum} = R_{DS}ON_{Q1}*I_O$$

The minimum achievable differential voltage depends on the output current and the ON resistance of the P-channel MOSFET. An important feature of the design in Figure 5 is that both the linear regulator and the converter share the same voltage reference and VA and V_O track each other over temperature, which is impossible to do with an external monolithic regulator.

A careful reader can see that the design in Figure 5 will not maintain minimum drop out voltage when the output of the converter is adjusted by ±10% or more of V_{OUT} Nominal. Beta Dyne took care of this minor detail and patented the design.

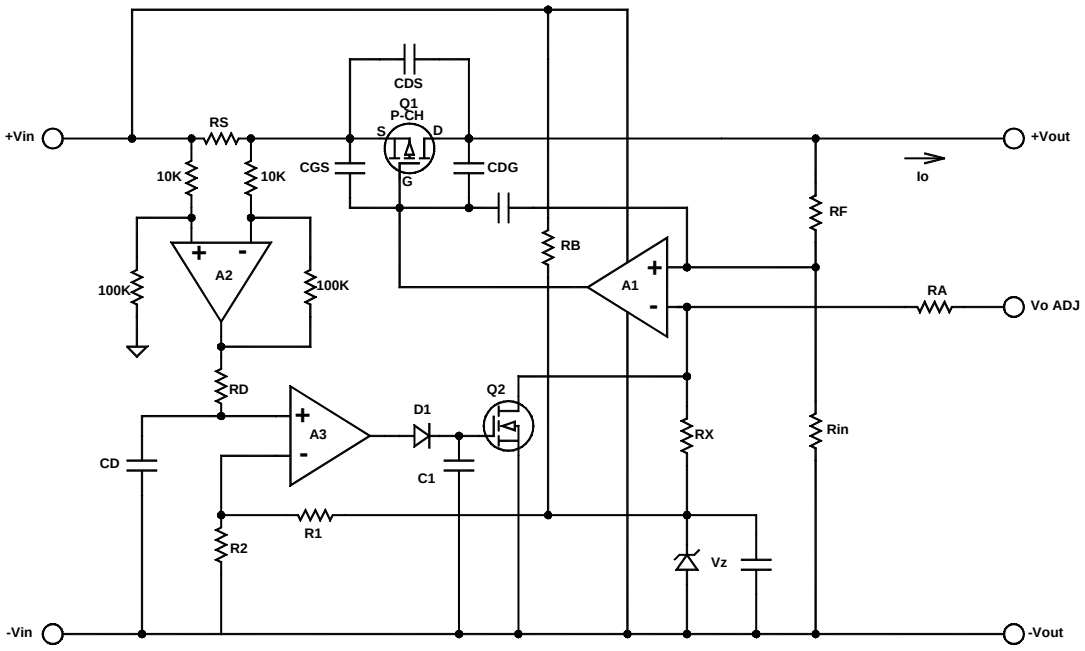

FIGURE 6. Low drop out linear regulator with short circuit protection

A low drop out linear regulator with short circuit protection is given in Figure 6. If thermal protection is required, a quad OPAM like LM324 can be used with a temperature sensor located close to Q1.

$V_O A2 = 10(RS*I_O)$

$$V_O = \left(\frac{RF}{R_{IN}} + 1\right)VZ$$

Even though power MOSFETs have some advantages such as low R_{DS} ON and low driving requirements, the parasitic capacitors can couple switching noise (output ripple of the converter) to the error amplifier and to the output of the regulator. In selecting Q1, one must take into consideration not only its R_{DS} ON, but also the parasitic capacitors, threshold voltage, and current rating assuming cost is not an issue.

Also, a PNP can be used in place of Q1, but a PNP has low current gain (hFE) typically from 80 at low I_O to I_O at 2–3A. One may argue that Q1 can be a Darlington Pair PNP with hFE of 1,000 or more. That would be correct but the dissipated power and the drop out voltage—which would be between 1.5V to 2V for the Darlington—would be 10 times higher than that of the P channel MOSFET.

NOTES:

· R2, R1 set the ouput current limit.

· RD, CD delay the activation of the output short circuit at turn ON to allow the regulator to charge large output capacitance.

· D1 C1 act as a peak detector with long Q2 ON period, a parallel resistor with C1 may be required to reduce the ON time of Q1.

· A1 must be able to switch within 1V of V_{IN} or a pull-up resistor must be installed between the gate and the source of Q2.

HIGH-VOLTAGE LINEAR REGULATORS

A fixed-input, high-voltage linear regulator is given in Figure 7. When designing high-voltage regulators, one must be careful in the selection of components.

In Figure 7, the error amplifier LT1006 is operated with 60µA supply current and the voltage reference bias is approximately 100µA (LM385-2.5V). Both the reference zener D2 and overvoltage protection zener D3 with the error amplifier are biased through the 2.5MΩ resistor.

All three N channel MOSFETs Q1, Q2, Q3 must be rated higher than V_{IN} Max, in this case 600V. Transistor Q2 provides output current limit while D1 protects Q1 from overvoltage between gate to source.

The power rating of all components must be calculated under worst case conditions and Q1 must be installed on a heat sink especially if V_{OUT} varies form 10V to 500V. When the input voltage of the regulator must be variable, say from 100Vdc to 550Vdc, high voltage current sources can replace the bias resistor R1, R2, R3. Also, take a look at STMicroelectronics' high-voltage regulators VB408 and VB409, which have 400V and 580V input respectively. They may work in your application.

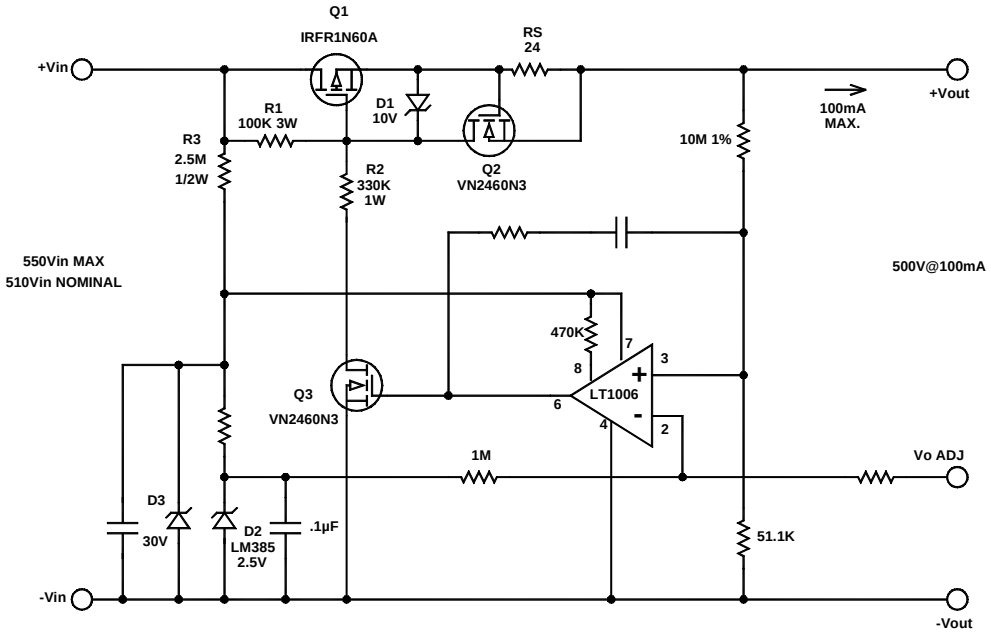

FIGURE 7. 50W fixed-input, high-voltage linear regulator

CONCLUSION

A common misconception in the industry is that if all the components designed in a system pass different agency standards for radiated and conducted noise, the system will pass the required noise standards.

WRONG! A compliance certificate tells you that you have a unit that, under specified conditions, will generate a specific amount of noise. An uncertified converter may very well have better noise performance and be more cost effective for your system.

Take into consideration the power requirements of a system during the feasability study and not after the design phase. Do not try to find a converter that meets your needs at the last minute. Follow the manufacturer's design guidelines and take into consideration not only EMI/RFI performance of the converter, but also the operating environment and more importantly the factor under your control: the layout of your system. This will reduce the design time, test cycle, and time to market of your product.

REFERENCES

1) Advances in Switched-Mode Power Conversion, Vol. I, II, III by R.D. Middlebrook and Slobodan Cuk
2) Switch-Mode Power Supply Handbook by Keith Billings
3) Transformers for Electronic Circuits by Nathan R. Grossner