PARALLELING DC/DC CONVERTERS WITH OUTPUT SYNCHRONOUS RECTIFIERS

FEATURING THE POWERWATT 75W DC/DC CONVERTER

DC/DC converters with synchronous rectification output are known for their ability to source or sync current in order to keep their output voltage constant. Depending on the application this can be considered as an advantage or disadvantage. It is an advantage in applications such as DDR RAM (Double Data Rate), where the converter provides the $1.25V_T$ voltage. In this application, the converter must source and sync current through the termination resistors of the DDR RAM modules. When the same converter must be connected in parallel with other (same type) converters, the synchronous rectification can become a liability if careful layout and output voltage trimming are not employed.

Output trimming to within 1mV to 5mV of the nominal output voltage for each parallel converter used will reduce or eliminate the tendency of the lower V_O converter to sync current from the other parallel converter in order to bring the other outputs to its own (lower) voltage. Trimming the outputs is the easy part; the most difficult and elusive parameter is the layout because other parameters will also affect the performance of the power system. The elusive parameters are the system operating temperature, the temperature coefficient (T.C.) of the reference diodes in each converter, and the efficiency of each converter.

The efficiency mismatch, which is in the range of 0.5% to 2% maximum, will contribute to the reference T.C. resulting in an increase or decrease of the output voltage. This assumes the system has no ground loops or other thermal problems, such as conducted or radiated heat from the load back to the converters.

In applications where more than 75W are required to supply a load, two or more 75W DC/DC converters can be connected in parallel to supply 150, 225, 300W or higher. The 75W DC/DC Converter from our PowerWatt series has all the features required for paralleling and load share. The converter can be synchronized to an external clock and provides a sync-out signal (which can be used as the sync-in signal for the N+1 converter).

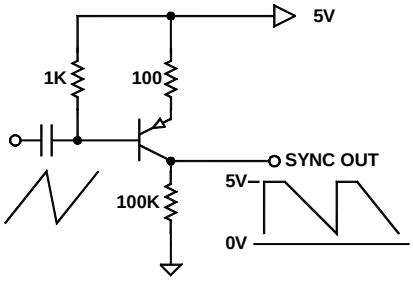

FIGURE 1

The sync-out signal is derived from the internal PWM clock as shown in Figure 1. When this signal is not used, very little power is wasted due to the 100kΩ load resistance. When sync out is used to drive the sync in of the N+1 converter, it must be reshaped to meet the requirements of the sync-in signal as described in the data sheet of our PowerWatt 75W DC/DC Converter (see Figure 6 in the data sheet). The sync-in signal must cross 2V High and 0.8V Low threshold. Therefore, by selecting a resistance between 1kΩ and 51kΩ as a load resistance for the sync-out pin (placed in parallel with the internal 100kΩ in Figure 1), the N+1 75W converter is synchronized to the N converter's frequency. The selection of the sync-out load resistance will force the N+1 converter to switch in phase (1kΩ) or out of phase (51kΩ) with the N converter. Two or more converters switching 180° out of phase results in lower output ripple and stress on the input capacitors (see Figures 2A, 2B and 4).

NOTE: Due to the high sync-in input resistance and relative high sync-out resistance, place the (1–51kΩ) load resistance close to the sync-in input at the N+1 converter. To avoid crosstalk, avoid crossing digital (sync-in, sync-out) signals, or use both sides or different layers of the PCB. Place the input capacitors for each converter as close as possible to the input pins and use a "star" input ground connection (see Figure 3) for both input and output grounds.

Due to the high output current of the converter, we recommend a multilayer PCB with a minimum of 2 ounces of copper layers that match exactly the copper trace resistance from the output power pins to the load. In Figures 3A & 3B, three 75S3.3/48 converters are connected in parallel for 200W maximum output power.

For equal current (load) share in parallel-connected converters, proceed as follows:

1) Use a single point to connect all equal resistance copper traces from each positive output; and a single point to connect all equal resistance copper traces from each negative output;

2) The resistance from the output power pin can be used to compensate for any small output voltage mismatch. In this case, the sense pin of each converter is connected at the converter power pin close to the converter and not close to the load. The voltage drop in the parasitic resistance of the traces will improve system reliability and affect load regulation and efficiency;

3) During the PCB layout stage, try to match the power trace resistance for both power runs by using copper traces of the same width. Keep in mind that the resistance of the copper trace is inversely proportional to its width and thickness, and that copper has high positive resistance T.C.

An evaluation PCB for three 75W converters (75S3.3/48 from our PowerWatt series) was developed (see Fig-

ures 3A & 3B) with 2-oz. copper double-sided. All three converters were tested individually in the same socket under 50% load (3.3@10A) and the output voltage was measured at top of the converter. The V_{OUT} measurements were: Unit 1: 3.321; Unit 2: 3.318; Unit 3: 3.334V_{OUT}. Using the same unit at 10A output current, the voltage drop was measured from the top of the converter pin to the load for both positive and negative power paths. The resistance for each power run was calculated and given in Figure 3 as parasitic resistance. A series resistance of 0.005Ω 1% 2W was used as a current sense with two test points across it. Then the output current was varied from 10A to 60A.

Table 1 gives the output currents per unit under different loads. It is obvious that a low-load unit (Unit 3) contributes more current than the other two due to the fact that its output is 14mV higher. Also note that at any loading, the output current mismatch is less than 1A. Between 40A and 50A, or 67% to 83% of full load, the mismatch is approximately 0.5A.

I_o	≈10A	≈20A	≈30A	≈40A	≈50A	≈60A
I_O (U_1)	3.22	6.34	9.74	12.20	15.56	18.20
I_O (U_2)	2.90	6.42	9.88	12.56	16.19	19.00
I_O (U_3)	3.84	6.96	10.16	12.58	15.68	18.40

TABLE 1

Even though we (intentionally) did not practice what we preach, the system performed exceptionally well. It had 3.5% output current mismatch, did not exhibit any startup problems under full load, even under 25A step load. Under no load, Unit 3 provided the output current sunken by Units 1 and 2. The 0.005Ω to 0.00125Ω series resistors plus the parasitics provided the necessary voltage drops to balance all three outputs. No input current increase was observed with no load. No trim potentiometer was used in the test PCB and is not required if the system is loaded with 20% minimum load. As indicated in its data sheet, the 75W converter offers its best efficiency between 30% and 90% of full load. Therefore we recommend operating the system within those limits.

When better output current share is required we recommend TI's UCC 39002 load share controller or other TI load share ICs. Please keep in mind that even if one of these controllers is used at each unit, the same layout principles apply. Plus you have to accommodate the controllers' requirements, such as compensation, trimming, and series sense resistors.

In addition, all three on/off input pins were connected together and the system was tested for turn on/off delay with additional output capacitors up to 3000µF at 60A I_O (see Figure 6). When a 10,000µF capacitor was installed on the output—for a total of 17,600µF and 60A I_O—the system started to go into overcurrent protection and its turn on delay was erratic with a maximum 50mS delay. With 7,600µF of total output capacitance, the output ripple was 10mV (see Figure 2B). Higher capacitance will not contribute much in further ripple reduction, but it may prevent the system from turning on.

In conclusion, when paralleling DC/DC converters with output synchronous rectification for load share, the N+1 converters must have the following characteristics:

- Voltage outputs (V_O) must be within ±0.25% of V_{OUT} Nominal,
- Output power run resistance (layout) must be within ±20% of each other,
- Out-of-phase switching frequency synchronization reduces input and output noise.
- Do not operate the system without minimum load; use 20% of full load as a minimum load.

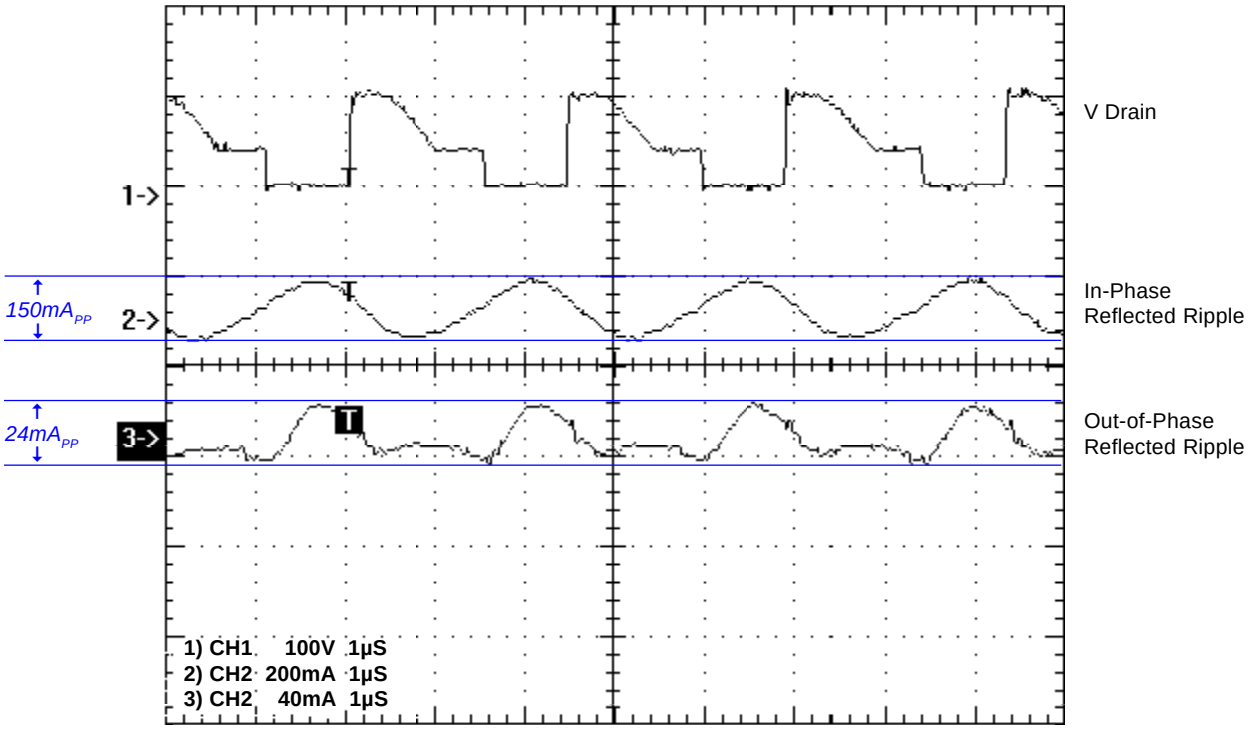

FIGURE 2A. Input reflected ripple for 150W converter (2×75W)

NOTE: Trace 1: Switching transistor drain voltage
Trace 2: Reflected ripple with in-phase synchronization
Trace 3: Reflected ripple with 180° out-of-phase synchronization
∴ 180° out-of-phase synchronization offers 6:1 reflected ripple reduction

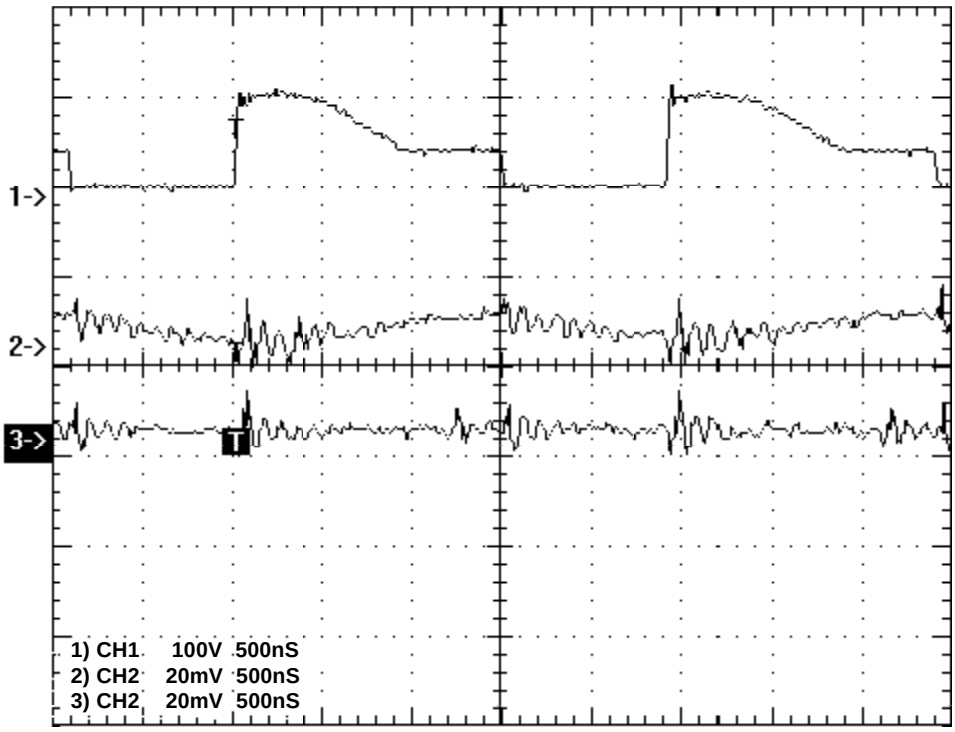

FIGURE 2B. Output ripple of 100W system (2×75S3.3/48 @ 30A)

NOTE: Trace 2 shows the output ripple of two 75W converters with in-phase synchronization and Trace 3 shows the effect of a 180° out-of-phase synchronization.

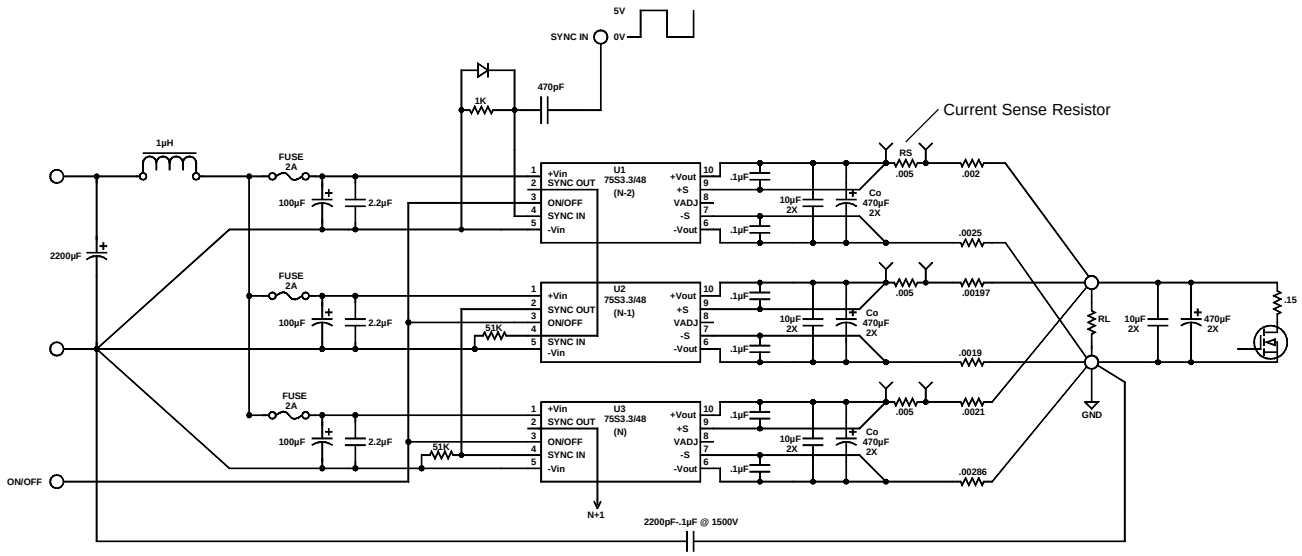

FIGURE 3A. Connection diagram for 200W converter with load current share

NOTE: A 0.005Ω 2W power resistor is used as a current sense resistor; all other values shown are parasitic copper run resistors.

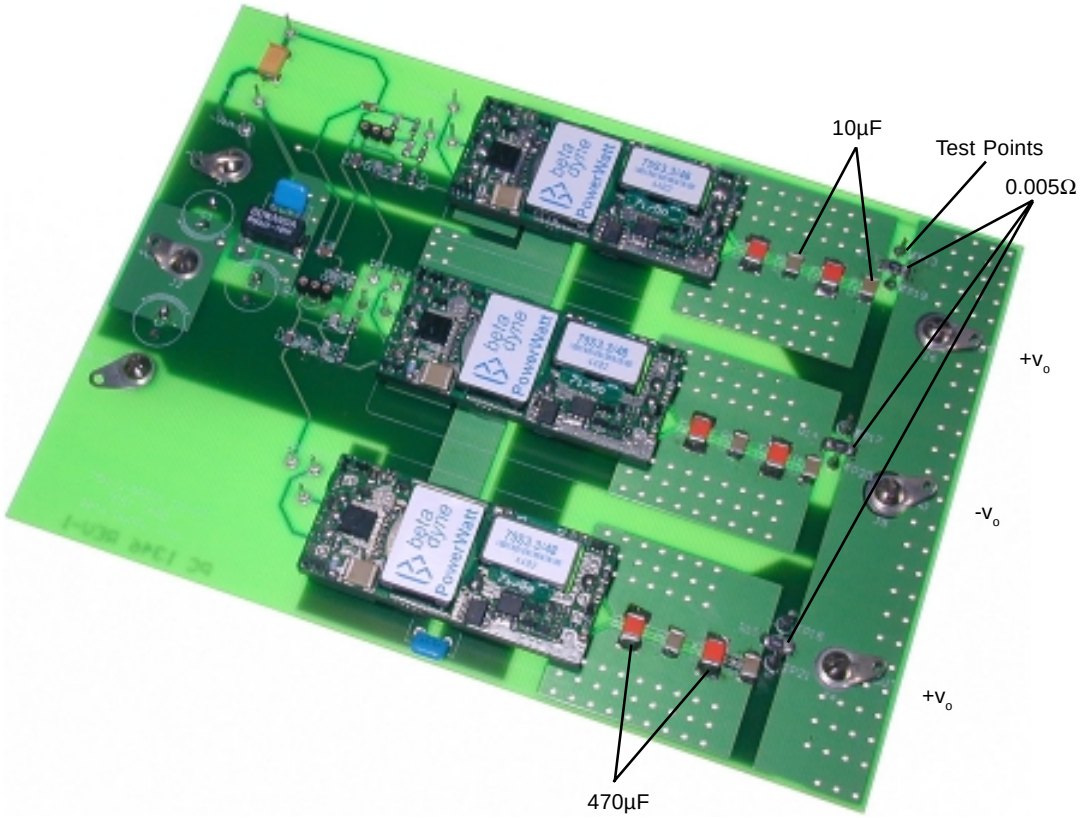

FIGURE 3B. Photo of evaluation PCB for three 75W DC/DC converters (75S3.3/48)

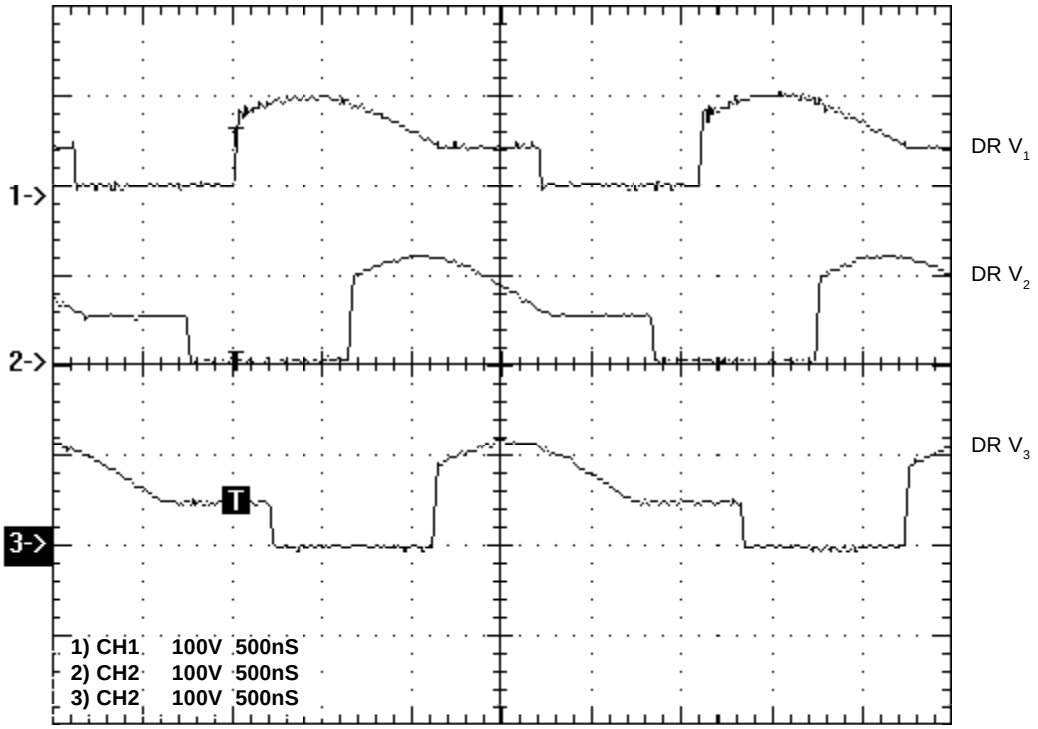

FIGURE 4. Drain waveforms of three 75S3.3/48 converters from the PCB in Figure 3

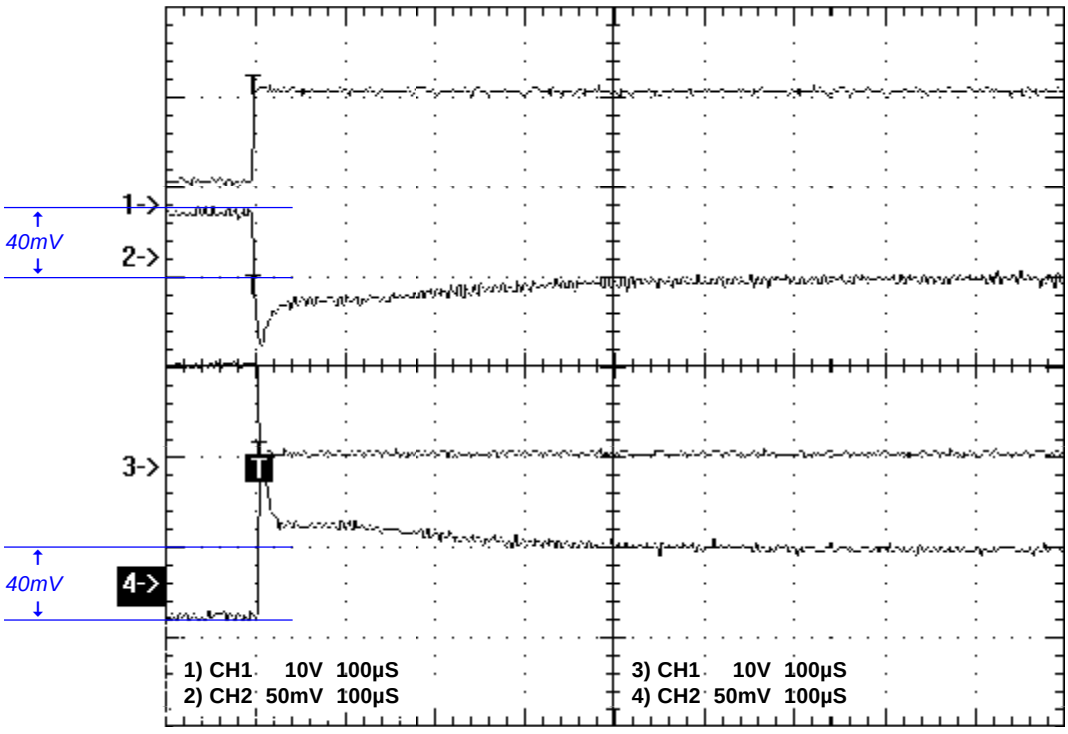

FIGURE 5A. Transient response of a 3×75W power system with 20A current step (30A to 50A to 30A) with a 0.005Ω series resistor at each output plus parasitics as shown in Figure 3

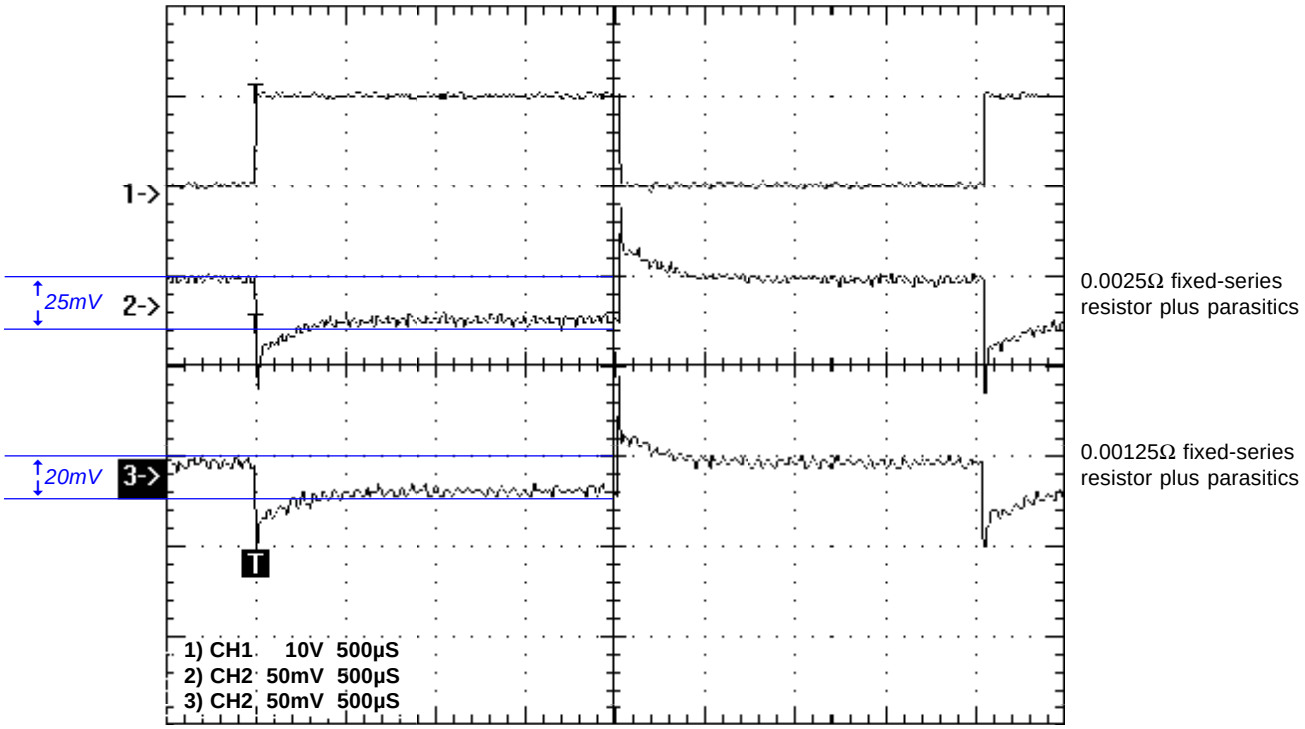

FIGURE 5B. Transient response of the system in Figure 3 with 20A load step (30A to 50A to 30A)

NOTE: Trace 2 is taken with 0.0025Ω and Trace 3 with 0.00125Ω fixed-series resistor. Notice the reduction of V_{OUT} step plus the fact that the sense pins of each converter are connected at the converter side of the fixed-series resistor and not at the load (see Figure 3B).

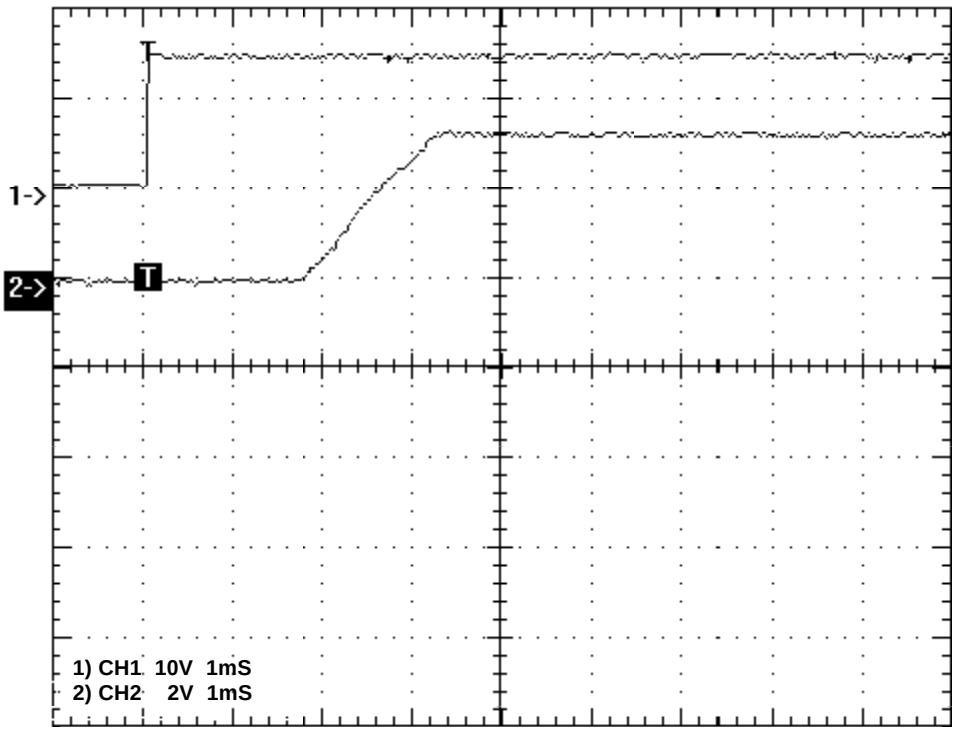

FIGURE 6. Turn on delay of 198W (3x75S3.3/48, V_o=3.3, I_o=50A)

NOTE:
C_o Total ⇒ 8×470µF = 7520µF tantalum + 8×10µF = 80 ceramics
C_o Total = 7600µF