Q25003

25-30W DC/DC Converter

2”×1”×0.45”

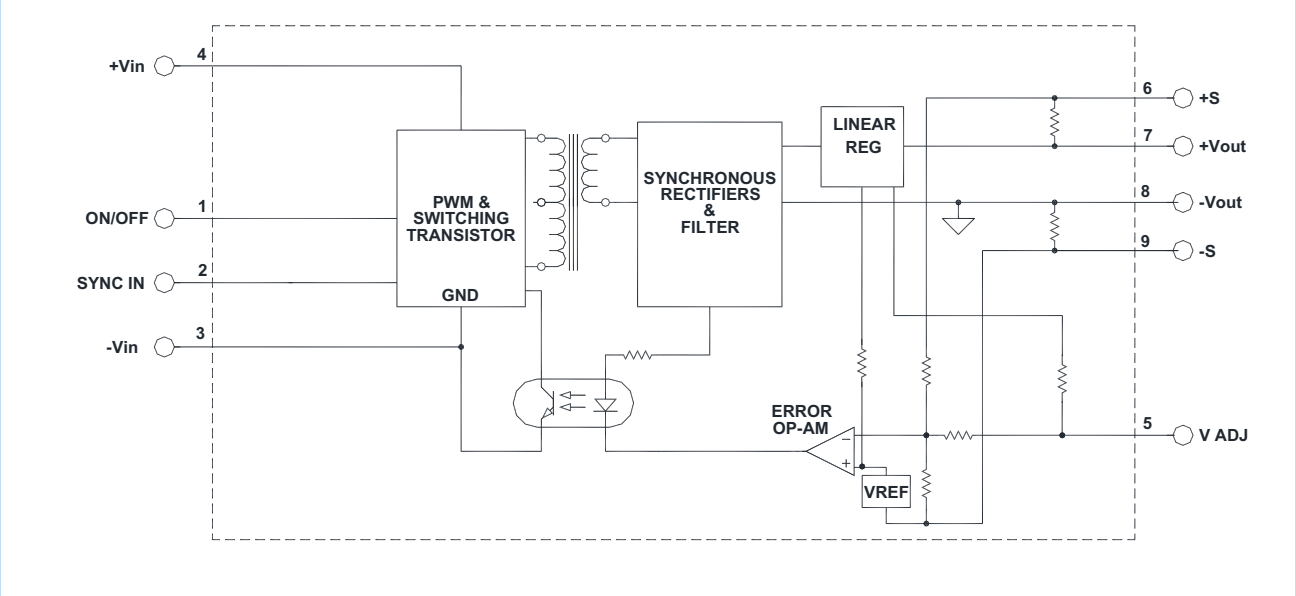
9.5-36Vin,6Vout@4.16A

Key Features

- Efficiency up to 85%
- Low output noise
- Six-sided shielding
- Output synchronous rectification
- Input-to-output isolation
- Soft start
- External synchronization
- Short circuit protection
- Thermal protection
- Industry standard pinout

Functional Description

The Q25003 is a 4:1 input range DC/DC converter that accepts 9.5-36Vin and provides 6.Vout at 4.16 A. The converter is designed to synchronize to an external clock. Output synchronous rectification followed by a very low dropout linear regulator makes possible to achieve up to 85% efficiency with less than 5mV output noise with external capacitors. Standard features include input undervoltage protection , external synchronization and thermal protection. The converter is packaged in a 2 x 1 x .45’’ metal case with six-sided shielding.



Typical Block Diagram

Electrical Specifications

INPUT SPECIFICATIONS

PARAMETER	CONDITION / NOTE	MIN	TYP	MAX	UNIT
Input Voltage Range		9.5	24	36	Vdc
Input Startup Voltage 24 V_{IN}		8		9	Vdc
Overvoltage Shutdown 24 V_{IN}		37			Vdc
Input Filter	Capacitor				
No Load Input Current			84		mA
Full Load Input Current			1218		mA
Input Surge Current (20µS Spike)				10	A
Short Circuit Current Limit	120% Of I_{IN} @ Full Load				
Off State Current			2.3		µA
Remote ON/OFF Control					
Supply ON	Pin 3 Open (Open circuit voltage: 10V Max.)				
Supply OFF		0		0.6	Vdc
Logic Input Reference					
Logic Compatability	TTL Open Collector or CMOS Open Drain				

OUTPUT SPECIFICATIONS

PARAMETER	CONDITION / NOTE	MIN	TYP	MAX	UNIT
Voltage			6.0		Vdc
Output Voltage Accuracy			1		%
Output Current	See Table 1 for capacitive loading information		4.16		A
Output Voltage Adjustment	See Figure 8		±5	±10	%
Ripple & Noise	For further reduction see Figure 3		20		mV
Line Regulation	Minimum V_{IN} to maximum V_{IN}		±.1		%
Load Regulation	NL to FL		±.1		%
Temperature Coefficient @ FL			.01	.02	%/°C
Transient Response Time	50% FL to FL to 50% FL, See Figure 1	100			µS
Short Circuit Protection	By Hiccup Technique				
Turn On Delay with Soft Start	See Figure 2				
Output Overvoltage Protection	None				

GENERAL SPECIFICATIONS

PARAMETER	CONDITION / NOTE	MIN	TYP	MAX	UNIT
Efficiency (at full power)			85		%
Isolation Voltage (1 min.), Input to Output	All models		1218		Vdc
Isolation Resistance			10^9		Ω
Isolation Capacitance			300		pF
Switching Frequency (FC)			300		kHz
External Sync Frequency (Fe)	See figure 6 & 7		400		kHz

PHYSICAL CHARACTERISTICS

PARAMETER	CONDITION / NOTE	MIN	TYP	MAX	UNIT
Dimensions (L×W×H)	2.00×1.00×0.450 in. (50.80×25.40×11.43mm)				
Weight	1.3 oz. (37g)				

ENVIRONMENTAL SPECIFICATIONS

PARAMETER	CONDITION / NOTE	MIN	TYP	MAX	UNIT
Operating Temperature Range (Ambient)	Industrial, See Note 2	-40		+71	°C
Storage Temperature Range		-55		+125	°C
Maximum Operating Case Temperature[1]				110	°C
MTBF	per MIL-HNBK-217F (Ground benign, +25°C)		1.1×10^6		hours
Shielding Connection	- V_{IN} for 24 V_{IN}				

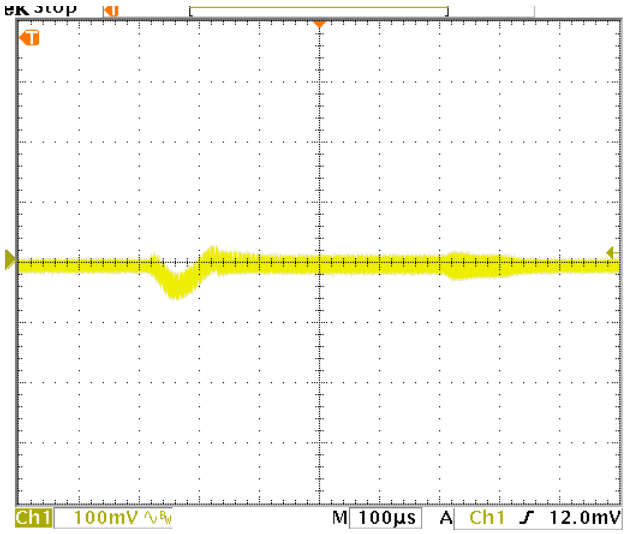


FIGURE 1. Transient Response at Vin=24, Iout changing from Full load to Half load on a Q25003.

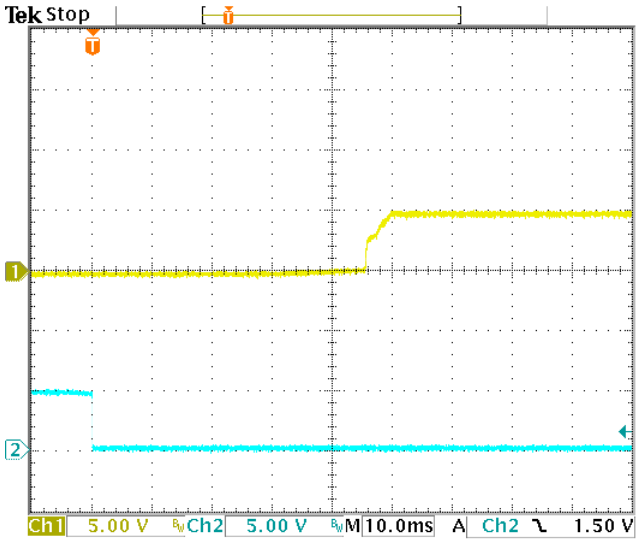


FIGURE 2. Typical Output voltage delay and rise time at Vin=24, Iout=5A using ON/OFF pin on the Q25003.

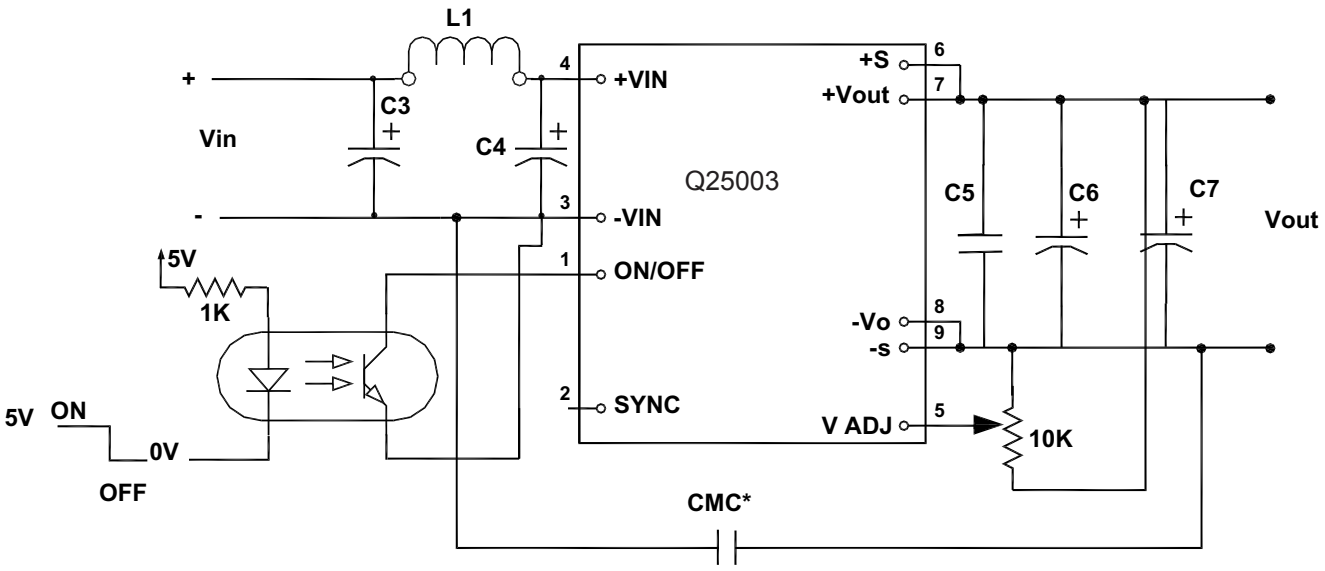


FIGURE 3. Typical connection diagram for Q25003.

Part list for Figure 1:
L1= 2.2µH
C3= 47µF@50V Electrolytic
C4=47µF@50V Electrolytic
C5= 1.5µF@25V Ceramic Capacitors
C6=47µF@20V Low Esr Tantalum
C7=180µF@16V Low Esr Tantalum

CMC*=Common Mode Capacitor
CMC= .01µF@Vcmc
Vcmc >= than required isolation, voltage can be up to 1500V dc max.

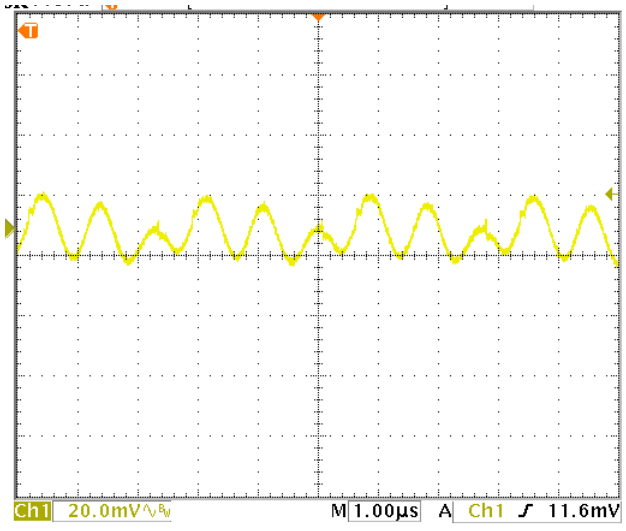


FIGURE 4: Output ripple of Q25003 with external cap of 1.5µF@25V on the output for C5 only.

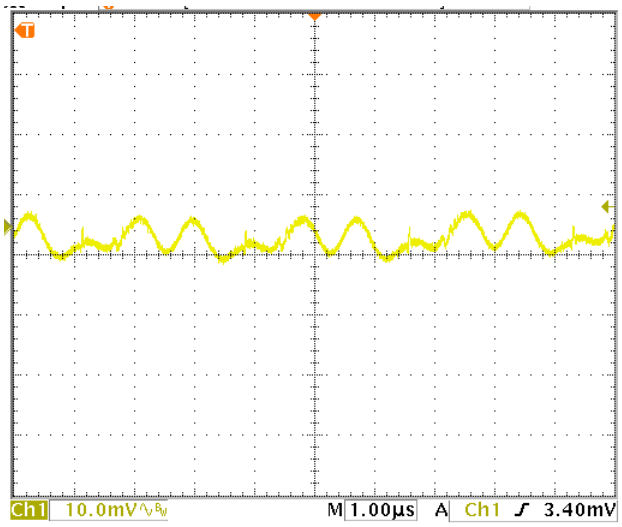


FIGURE 5: Output ripple of Q25003 with external cap of 1.5µF@25V (C5) and 47µF@20V (C6) on the output.

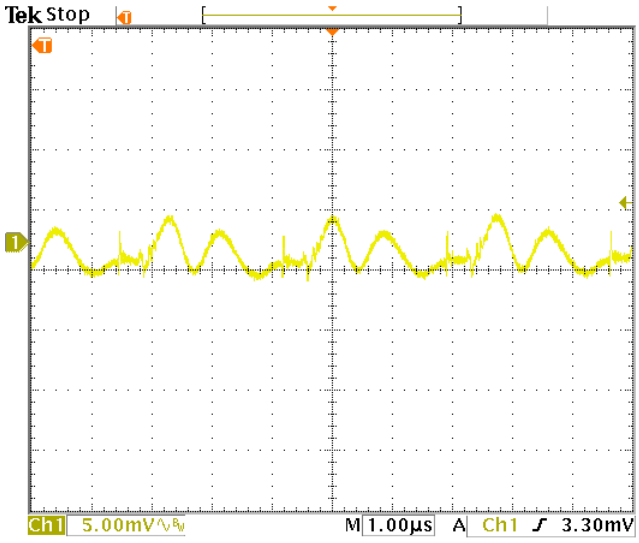


FIGURE 6: Output ripple of Q25003 with external cap of 1.5µF@25V (C5), 47µF@20V (C6) and 180µF@16V (C7) on the output.

EXTERNAL SYNCHRONIZATION

The SYNC pin can be used to synchronize the internal oscillator to external clock. An open drain output is the recommended interface between the external clock to the Q25 SYNC pin as shown in figure 7. The clock pulse width must be greater than 15ns. The external clock frequency must be greater than the frequency of the Q25.

Multiple Q25 converters can be synchronized together simply by connecting the converters SYNC pins together as shown in figure 8. Care should be taken to ensure the ground potential differences between the converters are minimized. In this configuration all the converters will be synchronized to the highest frequency device. The SYNC pin is a CMOS buffer with pull-up current limited to 200micro amps. If the external device forces the SYNC pin low before the internal oscillator ramp completes its charging cycle, the ramp will reset and another cycle begins. If the SYNC pins of multiple Q25 converters are connected together, the first SYNC pin that pulls low will reset the oscillator ramp of all the other converters. All converters will operate in phase when synchronized using the SYNC feature. Up to five devices can be synchronized using this method.

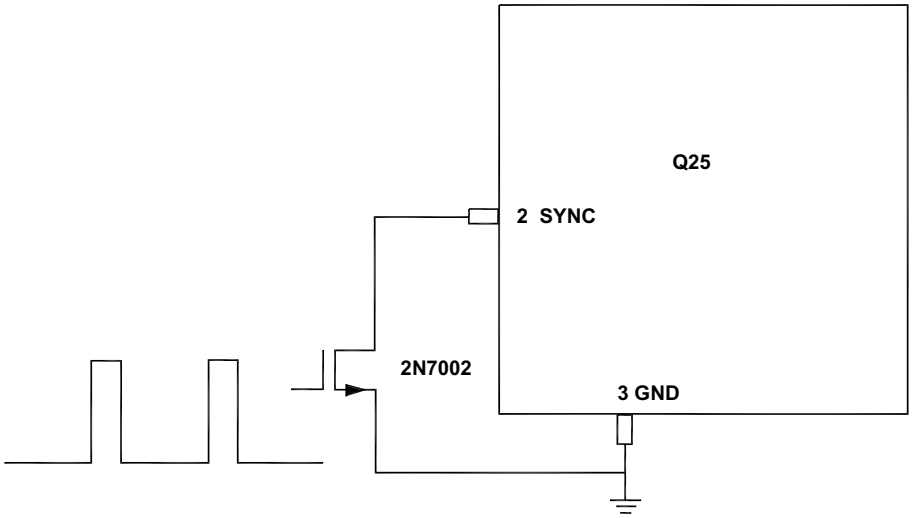


FIGURE 7. SYNC from external clock

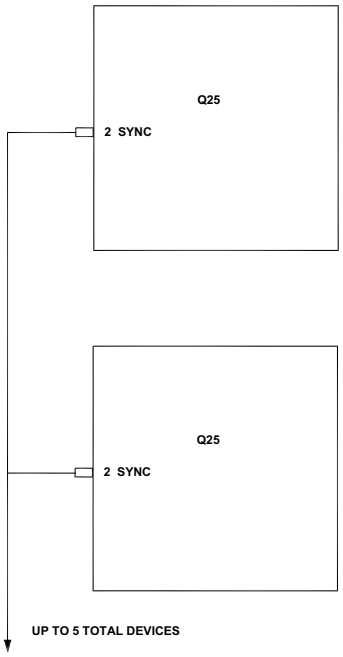
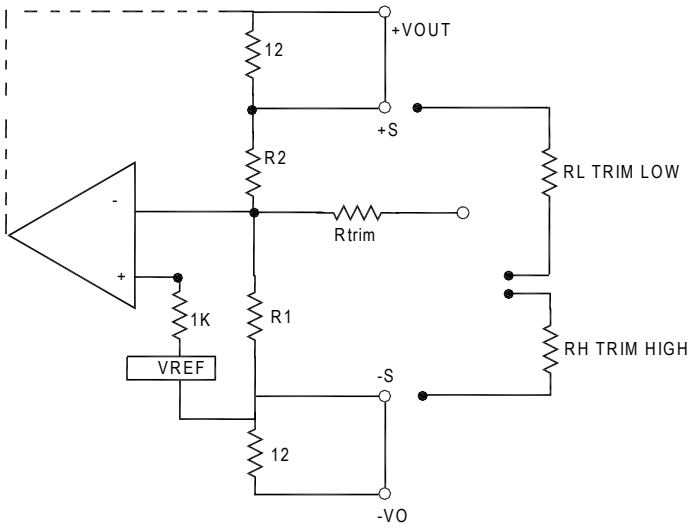


FIGURE 8. SYNC of multiple devices

Table 1. Capacitive Loading Tables with Output Current

V_{IN}(V)	I_{OUT}(A)	Capacitive Loading(µF)
9.5	5	470
24	5	2000
36	5	2000
9.5	4.16	1500
24	4.16	4000
36	4.16	4000
9.5	3.5	3000
24	3.5	7000
36	3.5	7000



$$RL = \frac{(Vo-Vref)R1*R2}{Vref(R1+R2) - VoR1} - Rt \quad \text{in k}\Omega$$

$$RH = \frac{R1*R2}{\left(\frac{Vo}{Vref} - 1\right)R1 - R2} - Rt \quad \text{in k}\Omega$$

VO	VREF	R2	R1	Rtrim
6V	2.5	4.99K	3.57K	9.53K

NOTE: Vo is the adjusted output voltage

FIGURE 8. Single Output adjustment equations.

Pin	Function
SINGLE	
INPUT	
1	ON/OFF
2	SYNC IN
3	$-V_{IN}$
4	$+V_{IN}$
OUTPUT	
5	V_{ADJ}
6	+S
7	$+V_{OUT}$
8	$-V_{OUT}$
9	-S

MECHANICAL SPECIFICATIONS