SYNCHRONOUS RECTIFICATION

Synchronous rectification (SR) is used in DC/DC converters when low output voltage is less than 5V and high current is needed. Synchronous rectification utilizes power MOSFETs to rectify the output voltage of the power transformer. These MOSFETs are synchronized to the converter frequency and perform more efficiently the rectification of the output voltage than rectifying diodes due to the low I×R drop through the channel. The N channel power MOSFET offers the lowest ON resistance and is relatively inexpensive.

In order to reduce the MOSFET ON resistance, semiconductor manufacturers parallel connect many higher ON resistance MOSFETs (or cells.) The parallel connection of cells not only decreases the ON resistance of the resulting channel but also parallel connects their parasitic capacitance.

Today, a typical N channel MOSFET has an ON resistance of 5 to 10mΩ V_{DS} 30V and a gate capacitance of 3300 to 6800pF. The higher parasitic capacitance of the power MOSFET limits its application to switching frequencies below 1MHz and requires high-speed, high-power gate driving signals to switch.

The power required to switch a given MOSFET is dominated by the power required to charge and discharge the gate to source capacitance. Given the switching frequency, the capacitance and the voltage magnitude the power required (dissipated) in the capacitance is given by:

$$P = V^2FC = Qgt*V*F \quad \text{Eq.1}$$

where P = Power in watts
V = Voltage in volts
F = Frequency in Hertz
Qgt = Gate charge in Coloumbs

The gate drive power plus any additional power for the semiconductors in the DC/DC converter is the overhead power needed for the converter to operate. Due to this overhead power, DC/DC converters with synchronous rectification exhibit the lowest efficiency at minimum load (typically 10-30% of full load) and their maximum between 60% and 90%.

In order to reduce this overhead power at minimum load, some DC/DC converter manufacturers employ additional circuitry to disable the MOSFET synchronous rectifiers by sensing the output current of the converter and allowing their parasitic diodes or external Schottky to perform the rectification. The additional circuitry may create more problems than it solves (see Application Note DC-001: Testing Transient Response in DC/DC Converters) and also affects the cost and the reliability of the converter (MTBF).

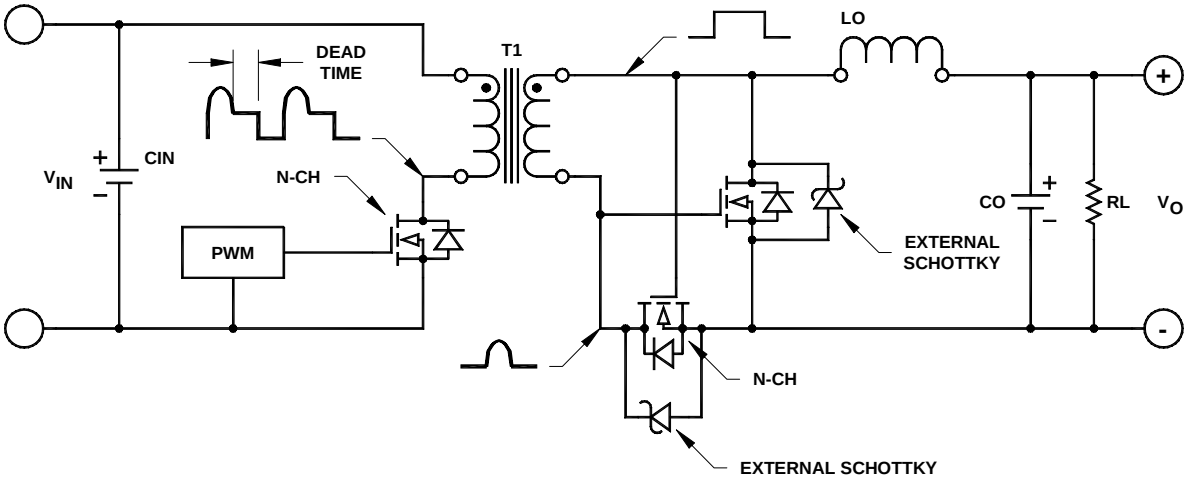

FIGURE 1

SYNCHRONOUS RECTIFICATION IN FORWARD CONVERTERS

Self-driven synchronous rectification (SR), as is shown in Figure 1, is driven directly by the secondary of the power transformer. It is the simplest but least efficient SR design due to the fact that the parasitic diodes in the MOSFET turn on before the gate voltage is developed at the secondary and during the dead time period of the switching cycle.

To lower the power dissipation on the parasitic diodes, designers have been using Schottky diodes in parallel with the MOSFET parasitic diodes. The self-driven SR can be used for low output voltages (2.5 to $5V_{OUT}$ range) and for 2:1 input range. For higher output voltages (V_{OUT} > 5V), additional circuitry is needed to limit the secondary gate-driving signal to lower values than the maximum V_{GS} for a given MOSFET.

PHASE LOCKED LOOP (PLL) SR

The PLL SR is more efficient than the self-driven SR, but it is also more costly and requires more area for the necessary components. The PLL SR has a local oscillator that locks on to the converter frequency and generates the needed driving signals for the MOSFETs (for more specific info, see IR1175 SR controller). The PLL SR offers design flexibility and eliminates the need for voltage limiters, however, their cost and component count is high.

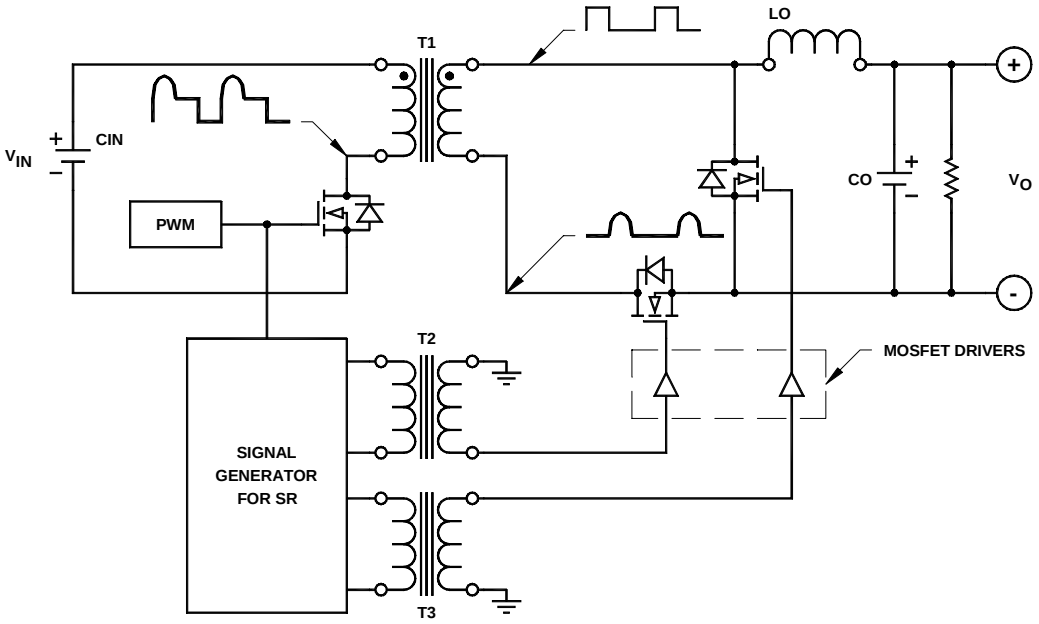

FIGURE 2

PRIMARY SIDE-DERIVED SYNCHRONIZATION

The PWM of the input side of the converter is used as a base to generate the driving signals needed for the output SR. These signals, which pass through an isolation transformer or high-voltage capacitor, are the inputs to a dual MOSFET driver circuit as is shown in Figure 2. The propagation delays are critical for the synchronization signal to avoid cross-conduction of the SR transistors.

FORWARD CONVERTER WITH ACTIVE CLAMP (AC) AND SYNCHRONOUS RECTIFICATION

In order to reduce the high voltage generated during the transformer core resetting period, forward converter designers employ demagnetizing windings, "snubbers," or active clamps. The demagnetizing winding will clamp the drain to the source voltage of the primary MOSFET switch and is useful for converters with ON duty cycles ≤ 0.50. Snubbers can be used for any duty cycle converter but they dissipate all the energy stored in their capacitors.

Forward converters with an active clamp use an active device, usually a MOSFET, to clamp the drain to the source voltage of the primary MOSFET to a predetermined voltage level by allowing the magnetizing current to circulate in the core during the reset period. The active clamp offers the following benefits: a reduction of the drain to source voltage of the primary switch through a reduction of the V_{DS}*I_P power and a minimization of the dead time period of the forward converter. However, it also requires additional circuitry and careful timing (see T.I. UCC 3580 PWM for more info.) An example of a forward converter with an active clamp is shown in Figure 3. NOTE: Due to the active clamp, a square wave voltage is generated at both ends of the secondary of T1.

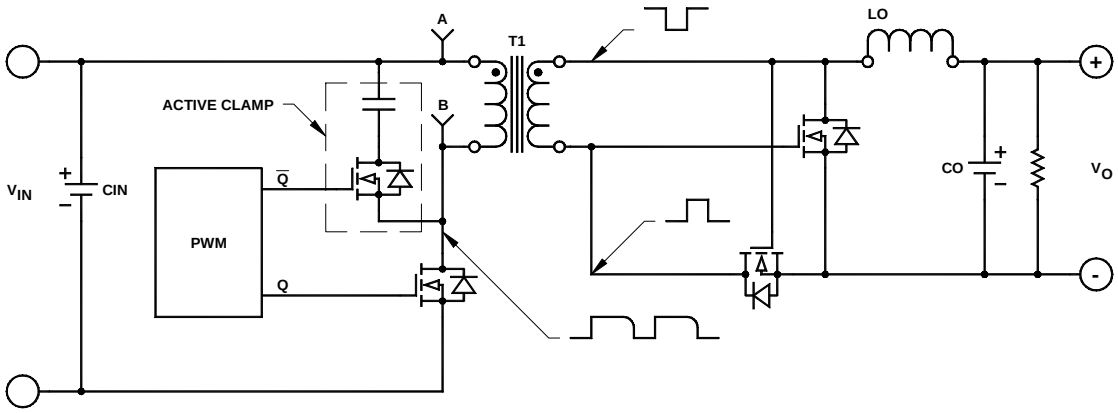

FIGURE 3