TESTING TRANSIENT RESPONSE IN DC/DC CONVERTERS

Most DC/DC converters use negative feedback to compensate for load and line variations. Usually a DC/DC converter is powered from a constant, low-impedance DC source that for all practical purposes does not have much of an effect on the transient load response of the converter.

The time required by the feedback loop to restore its output to its steady state is the transient response time. Different manufacturers specify different test conditions for obvious reasons. A transient response test can reveal the quality of the compensation of the feedback loop and its stability. When tested with transient loads, the output of under-compensated converters tend to oscillate, while the output of over-compensated converters take a long time to return to a steady state. Converters with an isolated output due to the isolation barrier delay exhibit longer transient response times than those with no isolation. Figure 1 below shows typical delay times of an optically-isolated flyback converter.

The total propagation delay in the feedback loop is the sum of all delays of the components used in the feedback loop. The above DC/DC converter (flyback) has a minimum delay of 5µS which implies that when a stepping load is connected to its output, the converter will start reacting after 5µS. The minimum delay time is NOT THE TRANSIENT RESPONSE TIME but a small fraction of it. In Figure 2, the two most popular isolated feedback loops are presented.

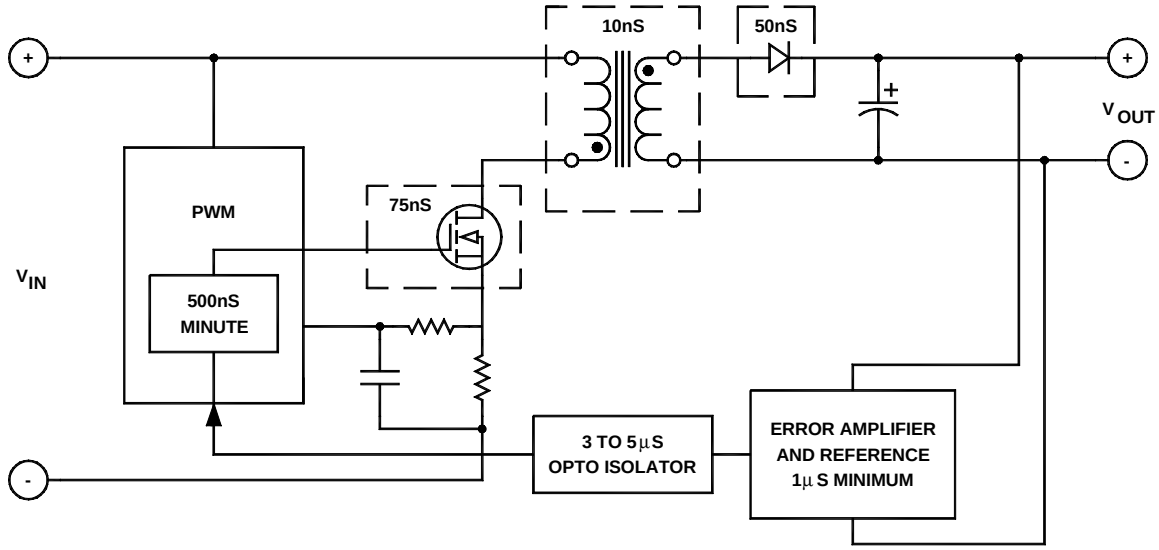

FIGURE 1. Delay times of an optically-isolated flyback converter

FIGURE 2 (Top). Opto-isolated feedback loop

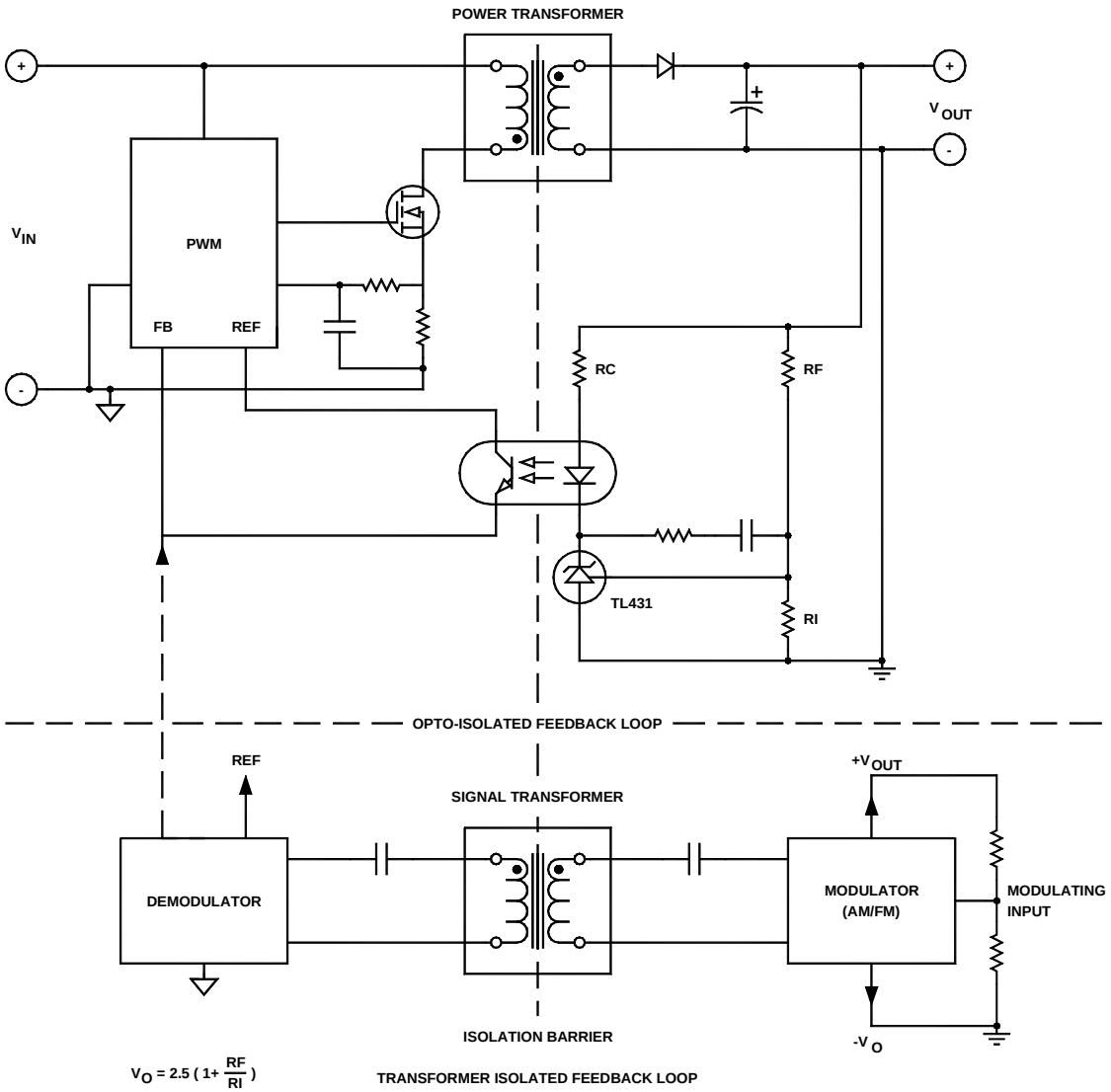

FIGURE 3 (Bottom). Transformer isolated feedback loop

After the minimum delay time, the PWM will start to modulate the transistor's on time to correct any output changes and will take a few power transferring cycles to bring the output to its steady state. There are two places in the feedback loop where designers use to compensate or stabilize the converter. One is the error amplifier and reference at the output and the other is the error amplifier in the PWM at the input side.

A detailed analysis of all the components in the feedback loop is very complicated, even for computer simulations which at best produce approximations. The best way to see the transient response of a DC/DC converter is to test it.

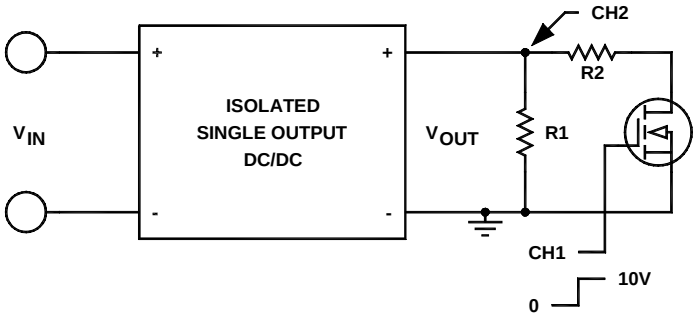

FIGURE 4A. Single output DC/DC converter

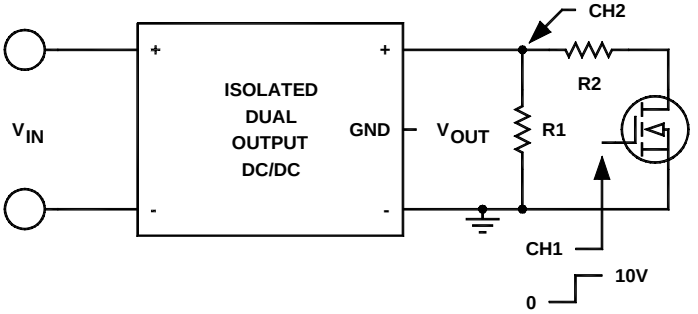

FIGURE 4B. Isolated dual DC/DC converter

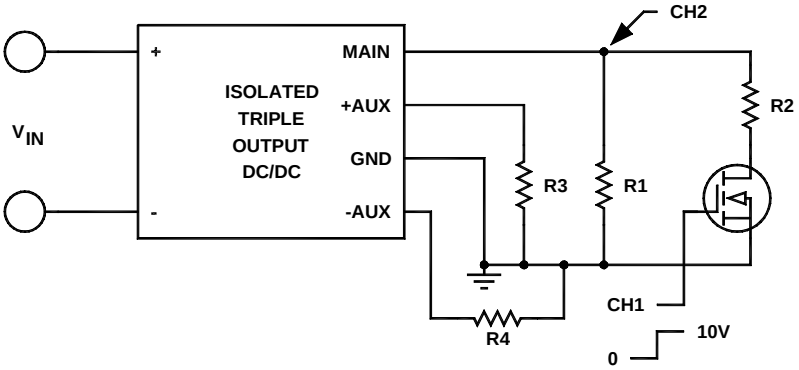

FIGURE 4C. Isolated triple DC/DC converter

The test circuits in Figures 4A, 4B and 4C show the load transient for a given converter.

Following the specification and test condition given by the manufacturer, set R_1 and R_2 to the required value and the square wave which drives the MOSFET from 0 to 10V amplitude and 500Hz frequency. The MOSFET connects R_2 to ground when its gate goes to 10V.

NOTE: Some manufacturers specify the maximum rate of current change over time (di/dt) during the transient load response test. In this case, an electronic load with adjustable current slew rate must be used in place of the MOSFET. A converter with limited di/dt indicates low output capacitance and long transient response time.

Assume that a manufacturer specifies the load step response of a 50 watt converter ($5V_{OUT}$ @ 10 amps) to be 100µS to within ±0.1% of V_{OUT} when the load changes from 50% to 100% to 50%. Based on this specification, if we set $R_1 = 1\Omega = R_2$ (Figure 4A), we will expect to see the output (5V) to settle within a window of ±50mV of its 5V output within 100µS. Figure 5A gives a typical transient response waveform.

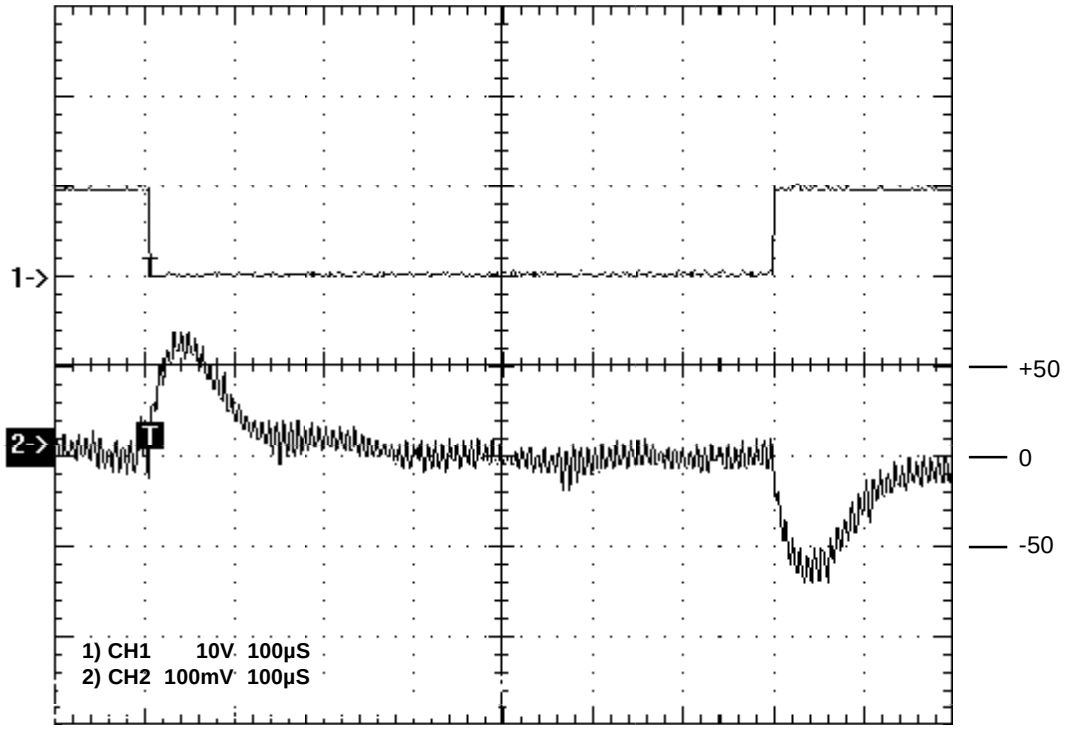

FIGURE 5A. Typical transient response waveform

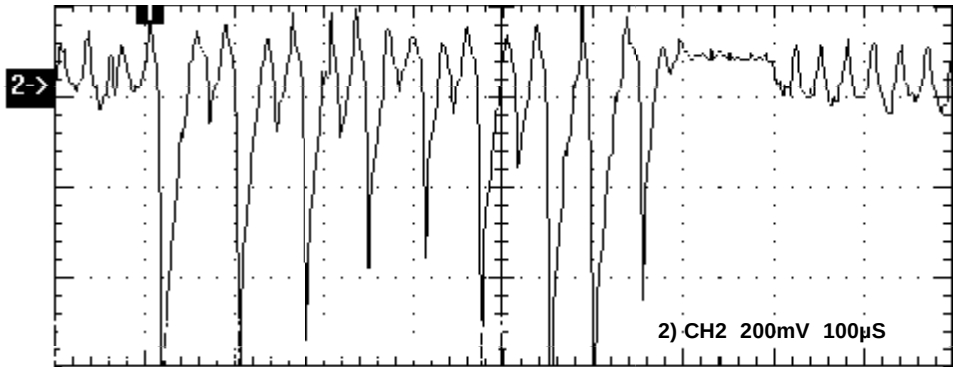

FIGURE 5B. Unstable waveform, 50% to 100% to 50% load step of a $5V_{OUT}$ converter (Exaggerated for demonstration purposes)

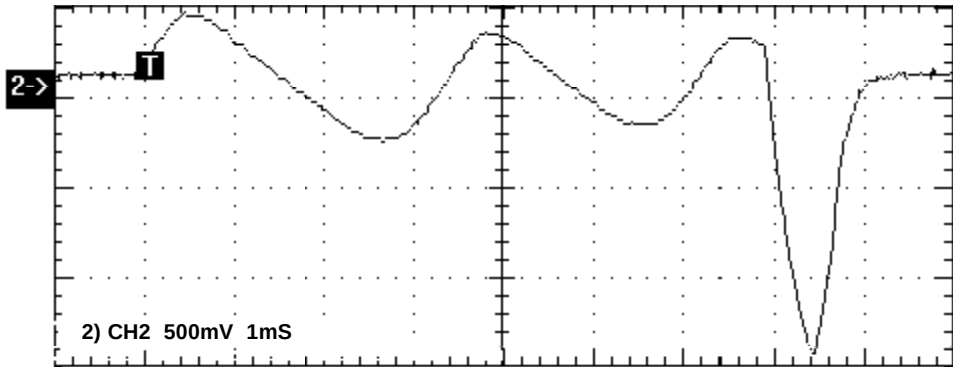

FIGURE 5C. Over comensated waveform, 50% to 100% to 50% load step of an over compensated $5V_{OUT}$ converter; NOTE: the negative transition is 1.8V, (Exaggerated for demonstration purposes)

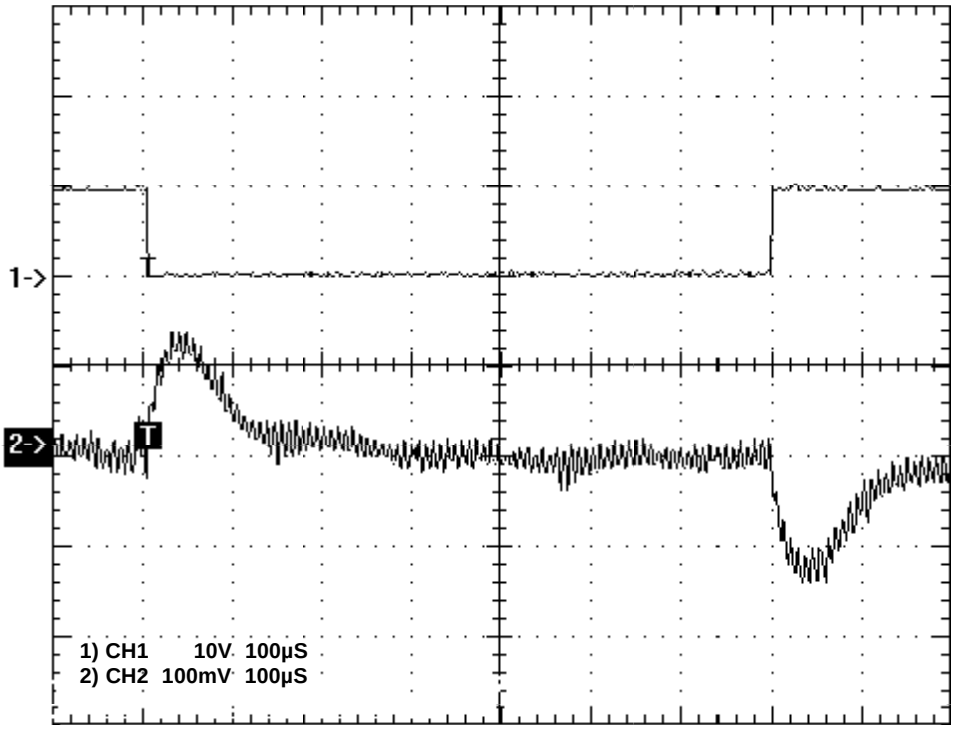

FIGURE 6A. Transient response 50% to 100% to 50% load step of a $5V_{OUT}$ over compensated converter

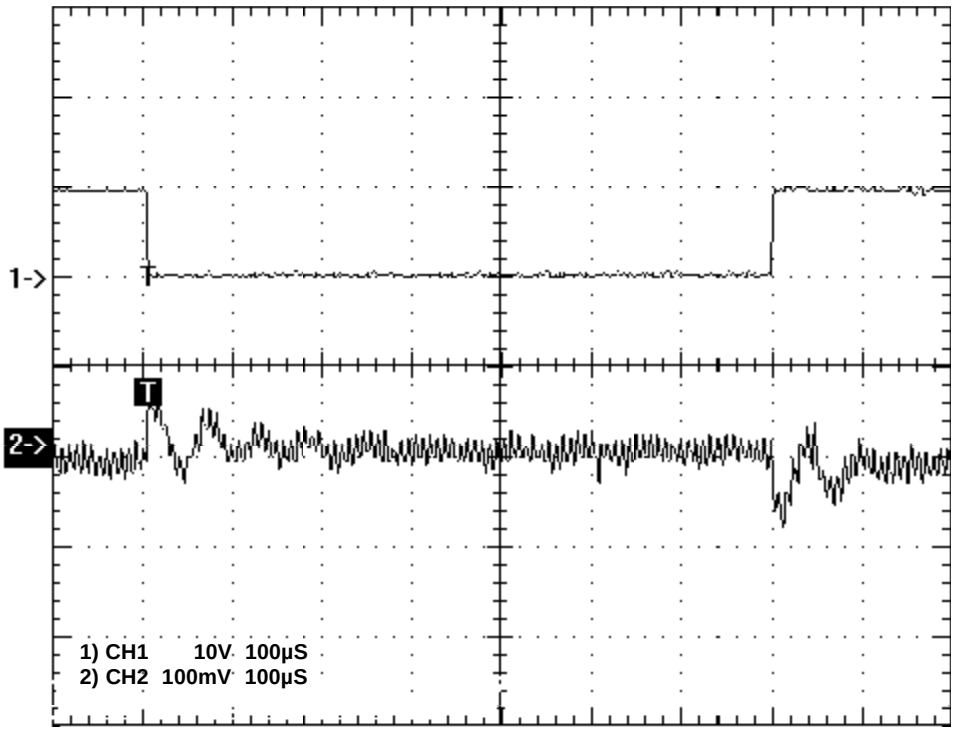

FIGURE 6B. Transient response 50% to 100% to 50% load step of a $5V_{OUT}$ under compensated converter

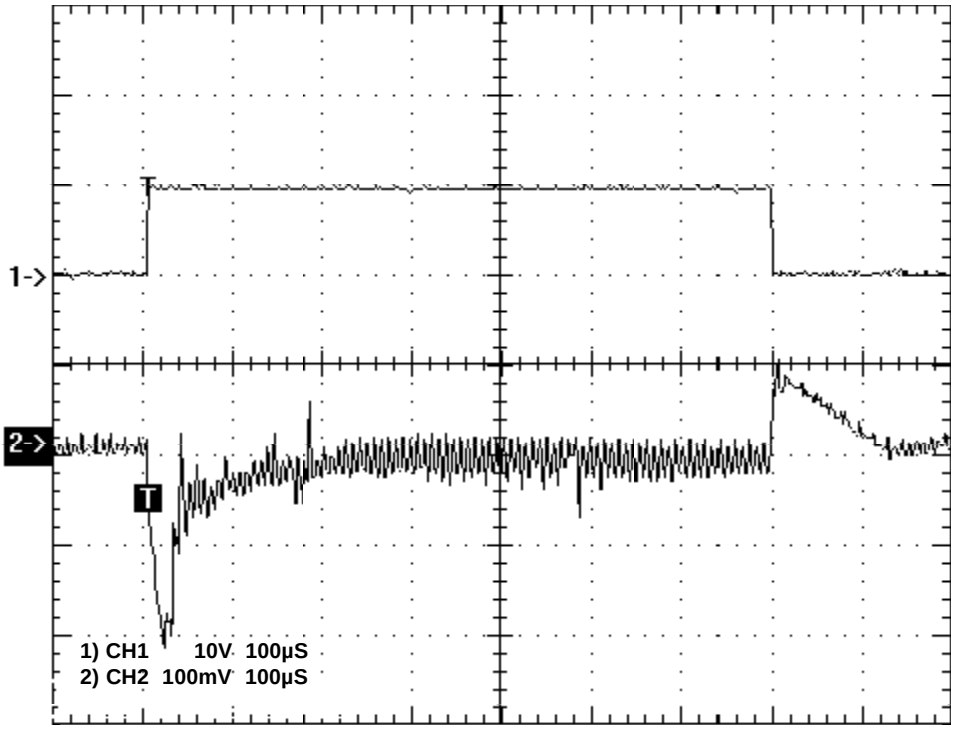

FIGURE 7A. Transient Response 25W 10% to 110% to 10% of Beta Dyne 25S005/24

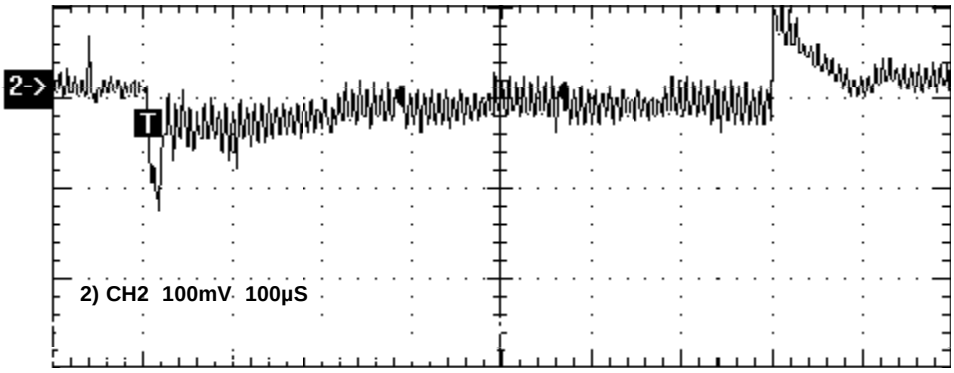

FIGURE 7B. Transient Response 25W 20% to 120% to 20% of Beta Dyne 25S005/24

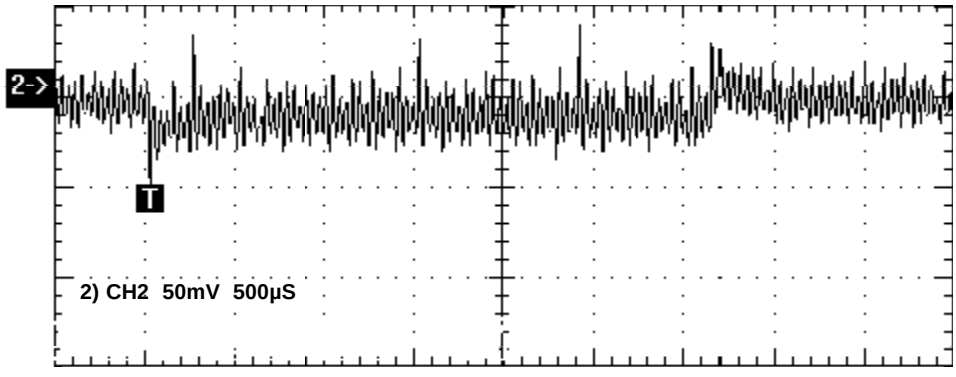

FIGURE 7C. Transient Response 25W 50% to 100% to 50% of Beta Dyne 25S005/24

The negative transition of the output occurs when R_2 is connected in parallel with R_1 through the MOSFET and the positive transition is due to the disconnection of R_2. During the negative transition of V_{OUT} (R_1//R_2), the output load is powered only by the output capacitors and can go as low as 4.5V if a small capacitor is used for the output filter. The converter's feedback loop will respond to the load change after its minimum delay time and it will start to deliver more power to its output to restore the charge in the output capacitors and the additional load R_2.

In Figure 8, note that during the first 7.5µS after the transition, the ripple waveform does not change in amplitude only shifts down 50mV discharging the output capacitor. After 7.5µS (2.5 power transferring cycles) the PWM starts to react by increasing its duty cycles to deliver more power to the output.

The ripple amplitude increases and at cycle 5 reaches 120mV. The sharp peak during cycles 4, 5 and 6 is due to saturation of the output inductor. This saturation increases the transient response time and over temperature of the converter making it unstable.

The transient response time in Figure 8 is 24µS; if the output inductor does not saturate, the transient resonse time could be 10µS. The amplitude of both the positive and negative transition and the settling time to within 0.1% of V_{OUT} will increase if the load is stepped from 20% to 100% to 20% as is shown in Figures 7A through 7C.

The amplitude of the negative transition can be reduced if additional capacitance is installed at the output of the converter, but it may increase the recovery time beyond 100µS. Excessive capacitance (e.g. more than 1000µF) on the output can cause the converter to go to short circuit protection mode at turn on even if the converter has a soft start circuit.

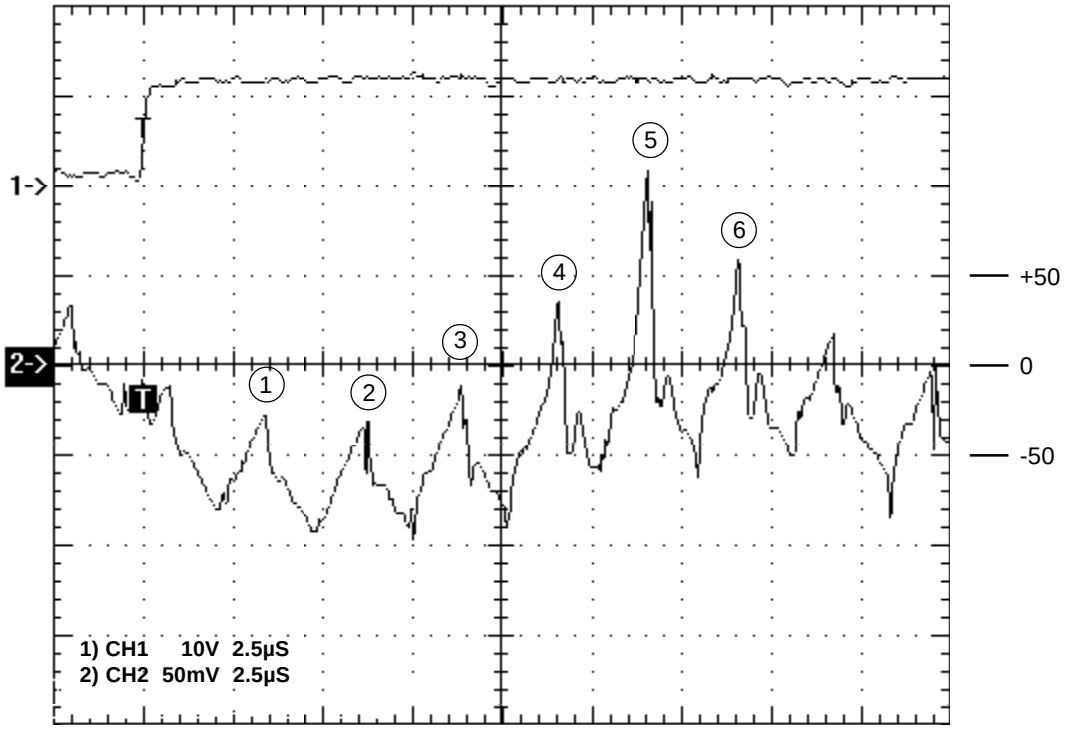

FIGURE 8. Output inductor saturation
(Cycles indicated by circled numbers)

When the MOSFET disconnects R_2, the propagation delay of the feedback loop and the closeness to the maximum duty cycle from the previous state causes an output overshoot which then over-charges the output capacitors.

The amplitude of the positive transition can be as high as 1V or more depending on the compensation of the converter. The feedback loop will turn the PWM off and no power will be delivered to the output until the overcharged output capacitor is discharged through R_1.

In a well compensated converter (Figure 5A), a decaying exponential waveform (R_1C_O time constant) is observed.

To test dual isolated output converters, the loads R_1, R_2 are connected between the positive and the negative outputs because the output error amplifier is monitoring the positive and negative outputs as is shown in Figure 8.

NOTE: The ripple and amplitude of the transient response for a dual output converter, observed between the positive and negative outputs, is double that at each output with respect to the output ground.

Testing triple output DC/DC converters is more involved if the auxiliary outputs are semiregulated and coupled through the core of the main output inductor. The set up in Figure 4C can be used to test triple output converters.

All outputs are loaded and the main output is tested for transient response. The transient response of the main output is reflected to the auxiliary output by a factor equal to the turn ratio of the main inductor to auxiliary inductor turns.

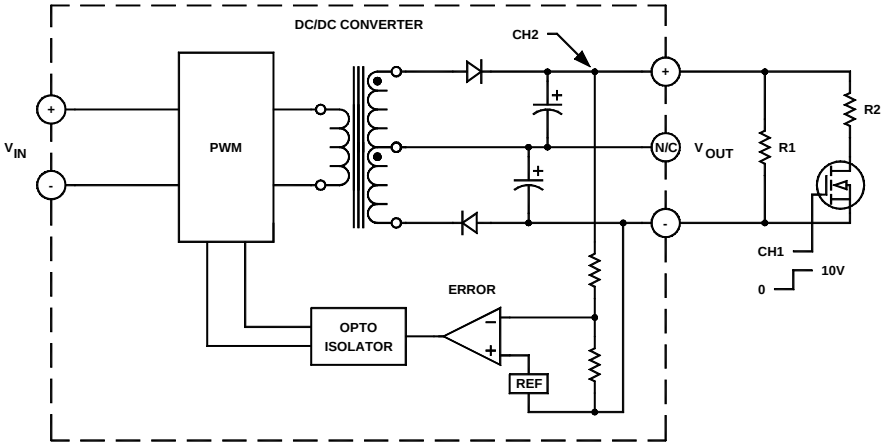

FIGURE 9. Typical output stage of a dual output converter and transient test response set up

TRANSIENT RESPONSE IN SYNCHRONOUS RECTIFICATION DC/DC CONVERTERS

In order to save power when the converter is operated at a low output power level, the synchronous rectification transistors are switched off allowing the output rectification to be performed through the transistor's parasitic body diodes or external, low-forward-drop Schottky diodes as is shown in Figure 10.

In Figure 10, the current sense amplifier monitors the output current and enables the timing and control circuitry when the output current exceeds a preset value. Therefore, the rectification scheme used in the output will not affect the transient response of the converter as long as the converter is operated above the minimum load set by the current sense amplifier. In rare cases where the output load is required to change from no load to a load above the current sense amplifier set current value, the enabling and disabling of the output synchronous rectification is very critical and must be tested. It may cause the output to go into short circuit protection and increase the transient response time.

The same potential problem may be observed in non-isolated, step-down converters with synchronous rectification where the PWM switches to "skip mode" operation during light loads to save power. For applications where the output load may switch from no load up to full load, use converters without "skip mode" or converters which enable the output synchronous rectification at turn on.

In conclusion, 1) a load transient response test in a DC/DC converter reveals not only the stability of the whole converter but also the internal circuit and component used for its output LC filter; 2) slow-responding converters are either over-compensated or incorporate the use of slow components in the feedback loop; 3) when a manufacturer specifies smaller than 50% load changes or slow di/dt, the converter is very slow and should not be used in fast-switching load applications.

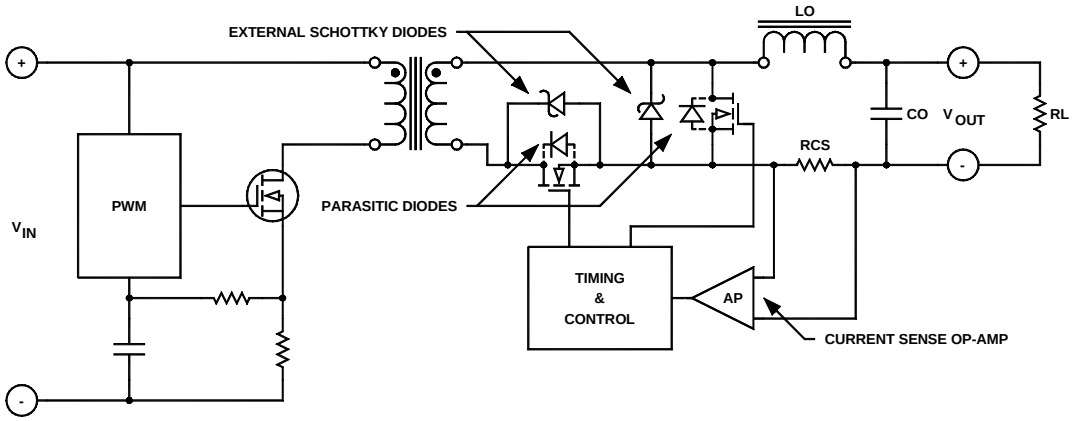

FIGURE 10. Typical forward DC/DC converter with output synchronous rectification