WHAT IS SO GREAT ABOUT SYNCHRONOUS RECTIFICATION?

SELF-DRIVEN SYNCHRONOUS RECTIFIER (SDSR)

Figure 1A shows a block diagram of a forward converter with an SDSR output. The SDSR consists of Q2 and Q3, which are directly driven from the secondary of the power transformer T1. The timing diagram and the associated voltage and current waveforms of Figure 1A are given in Figure 1B.

Referring to both Figures 1A & 1B, at t0 the PWM turns Q1 off. The current through Q1 drops to zero and causes the magnetic field in T1 to collapse and the drain to source voltage of Q1 to rise. Due to the parasitic capacitance of Q1 and the reflected gate to source capacitor of Q2 and the externally installed capacitance between the drain of Q1 and V_{IN}, the drain voltage of Q1 from t0 to t1 assumes a sinusoidal shape. The time period from t0 to t1 is also known as the core-resetting period during which the transformer core of T1 will return to its resting point on the B-H axis. The period t1 to t2 is known as the dead time period of T1. During this time, the core is reset and both gates of Q2 and Q3 are low, which forces both transistors off.

Even though both Q2 and Q3 are off, the current through L0 (IL) continues through the parasitic diodes in Q2 and Q3. When the parasitic diodes of Q2 and Q3 are forced by the output inductor to conduct the output current (IQ2, IQ3), the power dissipation (I0*VD) becomes excessive and reduces efficiency by 10-15%. The dead time period of the converter given in Figure 1A is proportional to the input voltage and to the output load. To reduce power dissipation during the dead time period, manufacturers of MOSFET power transistors have introduced the KEYFET transistors where the body diode is paralleled with a low drop Schottky diode. From t2 to t3, the PWM turns Q1 on, which then forces Q2 to turn on and Q3 to turn off.

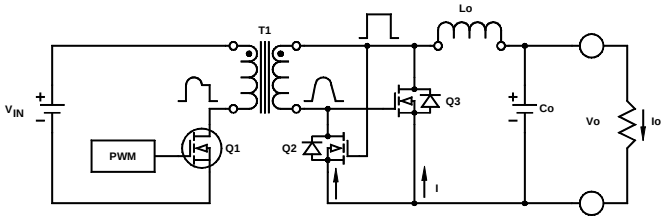

FIGURE 1A

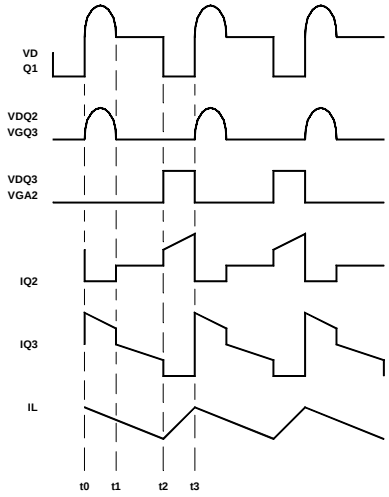

FIGURE 1B

As is shown in Figure 1B, the current through Q2 increases linearly from t2 to t3 and the sum of IQ2 and IQ3 is equal to IL at any instance form t0 to t3. It should be pointed out that at the beginning of t2 the parasitic diode of Q2 is forward biased and conducts the instantaneous IQ2 until the drain voltage of Q3 exceeds the threshold voltage of Q2 and forces Q2 on, thus short circuiting its parasitic diode. This instantaneous conduction of the parasitic diode (also known as a body diode) is very short in comparison to the dead time period (t1 to t2).

Forward converters with SDSR are simple, economical and can be cost effective only for minimum dead time applications. In other words, they are ideal for constant input voltage, constant load and single converter applications.

The converter in Figure 1A with the SDSR output cannot be connected in parallel for higher output power or redundant operation because the MOSFETs are directly driven from the secondary. Any voltage greater than the threshold of the MOSFETs (Q2, Q3) applied at V0 will turn the transistor on, which can result in two catastrophic events for the converter or the entire system:

1) A short circuit may occur at the applied voltage at V0, which may be the output of other converters, and;

2) Due to the applied voltage at V0, the switching action of Q2 and Q3 can produce catastrophic high-voltage spikes at the drain of Q1. Even when the converter is turned off and until the output capacitor is discharged by Q2 and Q3, the potential exists for catastrophic failure of Q1. Even though the converter in Figure 1A requires minimum parts, it is inefficient and can be used only for limited applications.

Additional circuitry can be used to eliminate all of the problems described above and even maximize the converter's efficiency, but will also increase cost and circuit complexity.

PARALLEL OPERATION FOR CONVERTERS WITH SYNCHRONOUS RECTIFIERS

Parallel connecting converters with output rectifiers is simple and, with the exception of some output voltage adjustments of the individual outputs for current sharing, is straightforward (see Figure 2).

It is obvious that at turn on or turn off, even if the turn on/off delays of each unit is different the output current has no path to ground except through RL. The diodes of the slower units will stay in reverse bias, allowing all the output current to go through RL. As long as all the converters possess a soft start feature and do not go into hiccup over current protection mode, the system of multiple parallel converters will start and deliver the required output power.

In converters with synchronous rectifiers, this is not the case! The turn on/off delays and synchronization of the synchronous rectifier is needed.

In Figure 3, the outputs of two converters with synchronous rectifiers are parallel connected. The control circuit of the MOSFET is given a block that can be an IC or all discrete components. If the control circuits are not synchronized, the converters in Figure 3 will run into problems at turn on. And even if they start, the system will not be reliable.

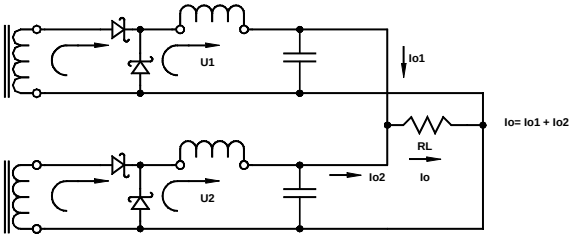

FIGURE 2

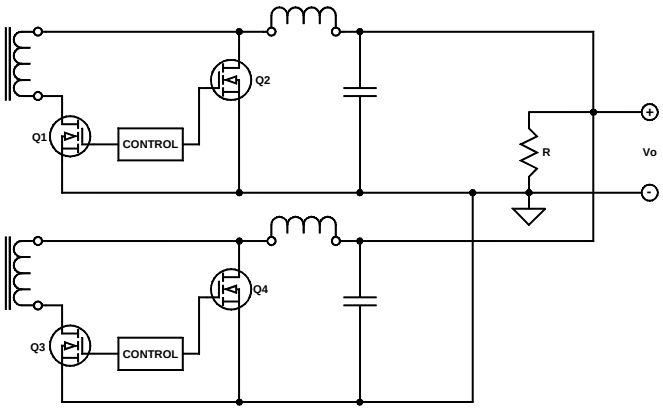

FIGURE 3

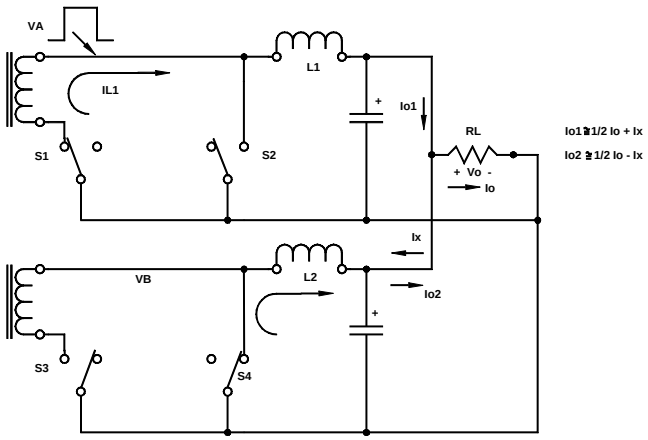

FIGURE 4

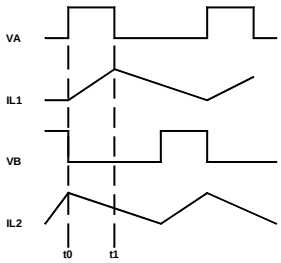

FIGURE 5

In Figure 4, the transistors of the synchronous rectifiers are replaced with switches and are shown to be out of phase. If the converters in Figure 4 had separate loads, the waveforms in Figure 5 would be observed. Note that at t0, IL1 increases linearly while IL2 decreases linearly. When the converters in Figure 3 are connected in parallel and are not synchronized, some of the output current will flow back into the other converter resulting in catastrophic failure of one of the SR transistors over time or the system will refuse to start.

Assuming for a moment that both converters are synchronized and is matched with the SR driving signal to within ±1nS, the converters must work perfectly and equally share the load current. But again this is not the case!

In Figure 3, the other variable that is not shown which can affect the SR timing is the negative feedback control loop in both converters. Under ideal conditions for both V01=V02, the synchronized PWM will provide equal pulse width for both converters. The power MOSFET used for SR's have very low RDS_{ON} (from 5mΩ to 10mΩ) and high gate to source capacitance (from 3300pF to 6800pF).

The high gate to source capacitance of the SR transistors dissipates power, reduces the transistors' switching speed and, under the best driving conditions, will switch in 50nS to 75nS. Under these switching conditions, the total synchronization error between the drivers for the SR's of the parallel connected units must be within ±35nS, under any condition such as line, load, temperature and feedback control loop response. Therefore, it is not practical to parallel connect commercially available DC/DC converters with SR output.

Do not operate these converters with no load or minimum load. The obvious solution to this problem is the elimination of a few variables. Beta Dyne has solved this problem using an old but reliable method of master-slave (M-S) configuration. The M-S approach eliminates the multiple feedback loops by forcing all the slaves to synchronize to a single digital signal generated by the master.

DC/DC converters with synchronous rectifiers need additional circuitry and careful timing especially for parallel operation. If they must be connected in parallel, use minimum load. For redundant operation, preload the converters before the ORing diodes with minimum load. For reliable operation and peace of mind, use Beta Dyne's master and booster converters.

In conclusion, DC/DC converters with synchronous rectifiers offer higher efficiency and power density.